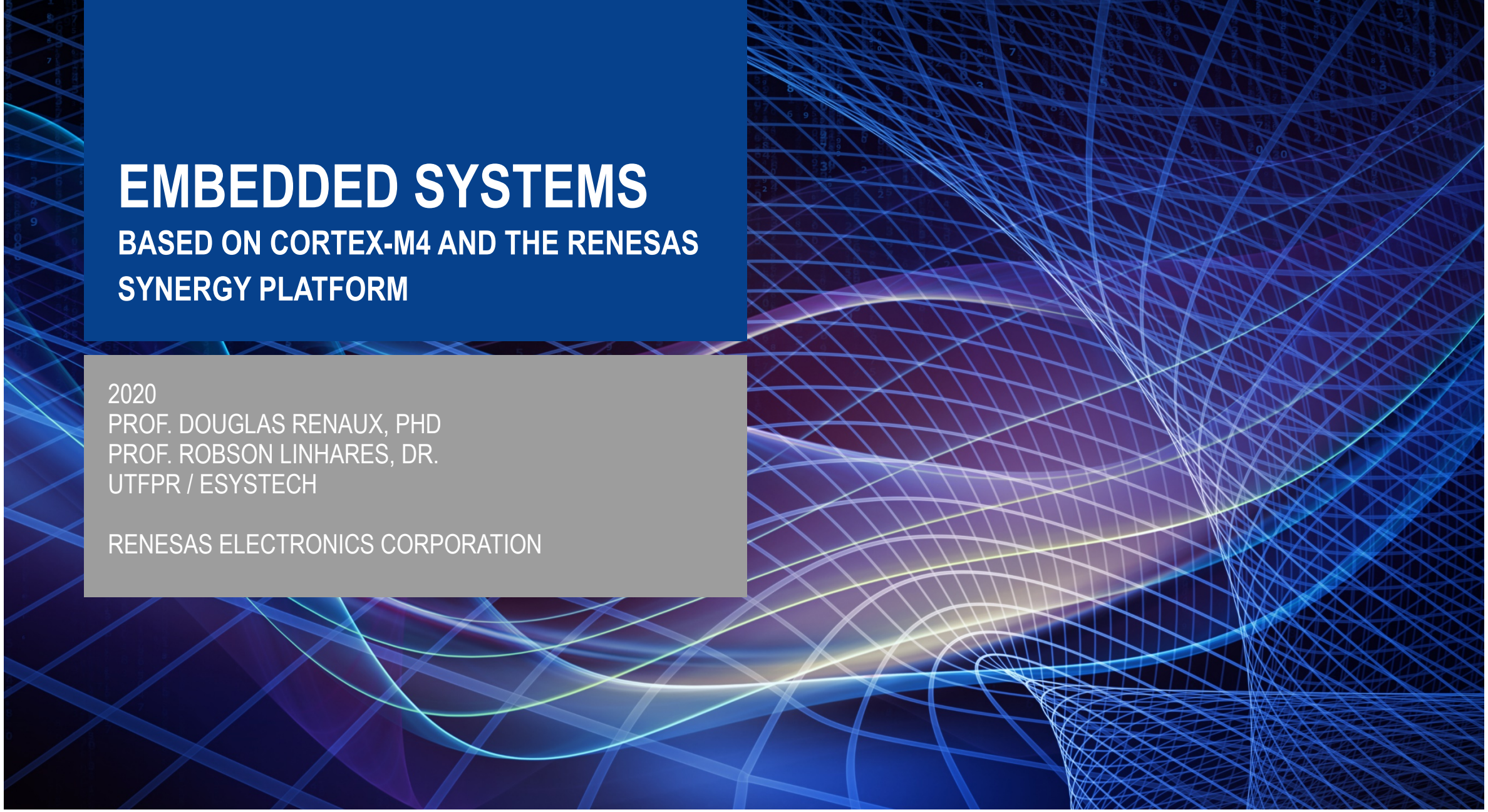

EMBEDDED SYSTEMS

BASED ON CORTEX-M4 AND THE RENESAS SYNERGY PLATFORM

2020
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LAB4 – TIMER DEVICE DRIVER

Objectives:

Use a GPT (General PWM Timer) to generate a 100 Hz rectangular waveform with a 25% duty cycle. The SSP components for the GPT are NOT to be used. Here, the student is to exercise the direct interaction with the GPT hardware.

LAB4 – TIMER DEVICE DRIVER

Learning Objectives:

- Study a hardware peripheral with the objective to develop its device driver
- Identify the relevant registers of a peripheral for a given application
- Design an algorithm of a device driver
- Evaluate alternatives of means to interact with the registers of hardware peripheral

LAB4 – TIMER DEVICE DRIVER

Activities:

1. Study the GPT (General PWM Timer of the S7G2 MCU)
2. Determine the sequence that the GPT registers must be programmed and the respective values
3. Design an algorithm to achieve the purpose
4. Implement and test

further reading for this Lab:

Renesas Synergy Software Package v1.7.5 User's Manual
r11um0140eu0106-synergy-ssp-v175

GPT HAL Module Guide
r11an0091eu0101-synergy-gpt-hal-mod-guide.pdf

LAB4 – ACTIVITY 1

Activities:

- S7G2 microcontroller's block diagram with indication of blocks of interest.

- Since the user's manual of the S7G2 has more than 2000 pages, it is important to keep focus on what is relevant to this project.

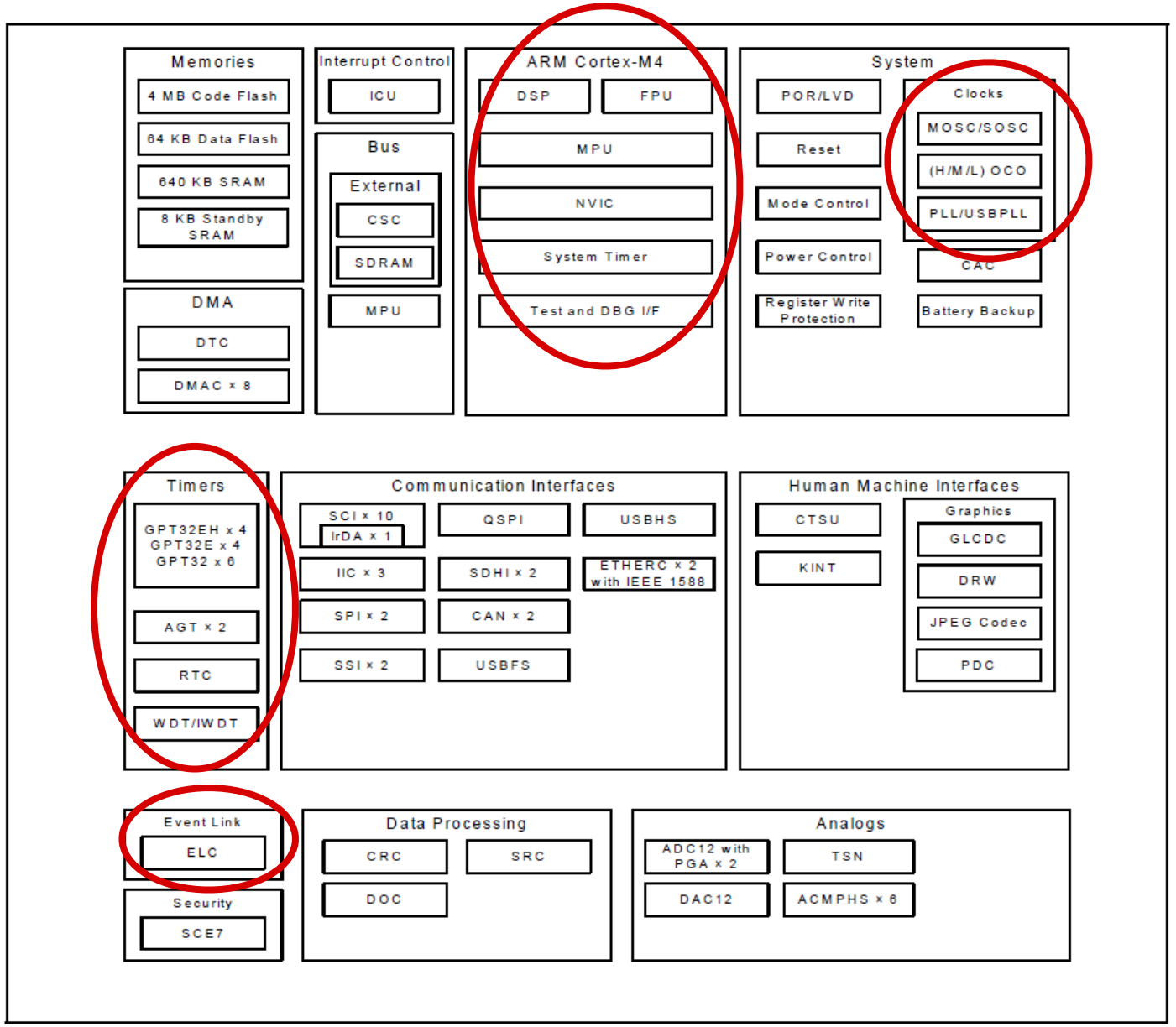
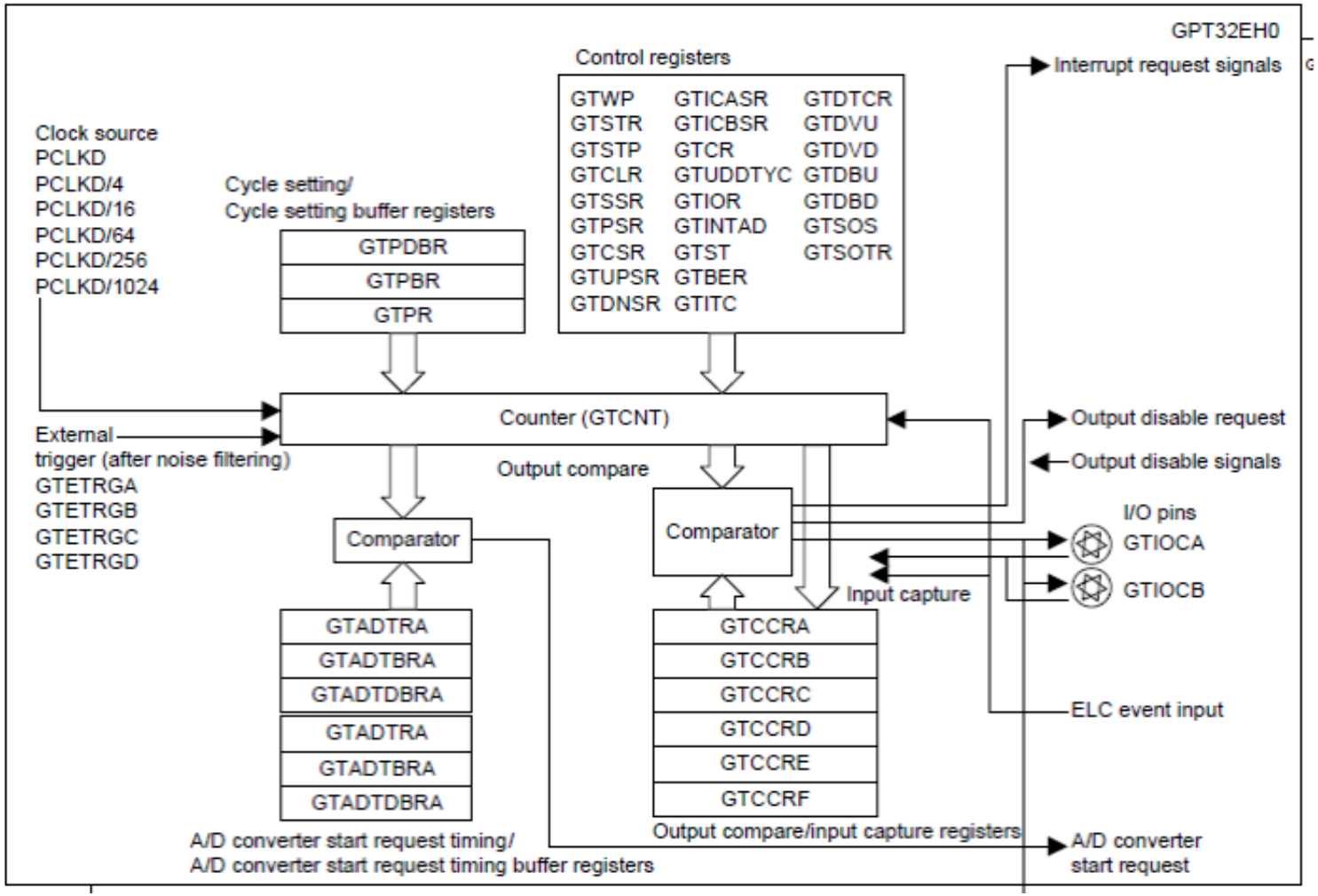


Figure 1.1 **Block diagram** source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 1

The block diagram of GPT (General PWM Timer).

- GPT characteristics:
- 32-bit counter
- counts up or down
- can generate interrupts
- can start an ADC conversion
- counts PCLKD pulses
- periodic or single-shot
- 14 channels, each is a 32-bit counter

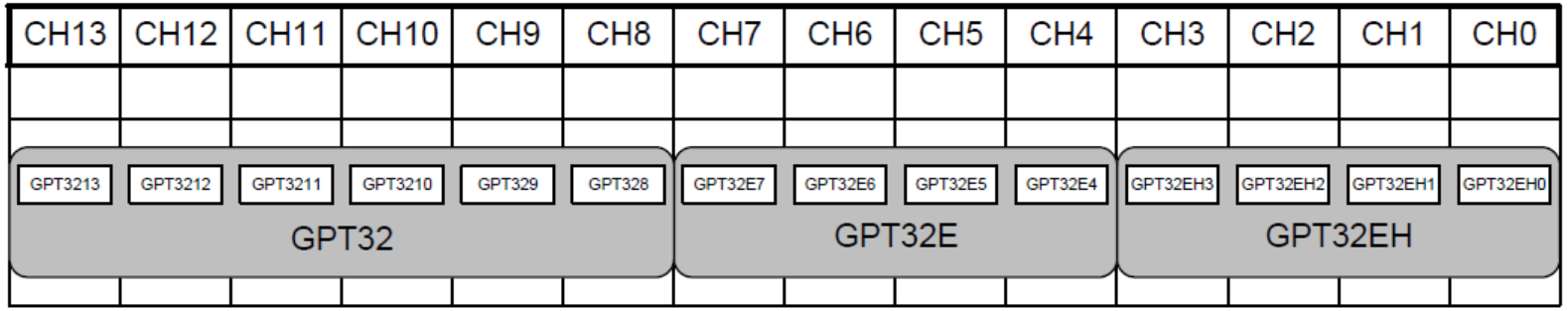


source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 1

The 14 timer channels are grouped into:

- 4x EH – enhanced high resolution
- 4x E – enhanced
- 6x – conventional



source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 1

Registers of the GPT

GTWP	: General PWM Timer Write-Protection Register
GTSTR	: General PWM Timer Software Start Register
GTSTP	: General PWM Timer Software Stop Register
GTCLR	: General PWM Timer Software Clear Register
GTSSR	: General PWM Timer Start Source Select Register
GTPSR	: General PWM Timer Stop Source Select Register
GTCSR	: General PWM Timer Clear Source Select Register
GTUPSR	: General PWM Timer Up Count Source Select Register
GTDNSR	: General PWM Timer Down Count Source Select Register
GTICASR	: General PWM Timer Input Capture Source Select Register A
GTICBSR	: General PWM Timer Input Capture Source Select Register B
GTCR	: General PWM Timer Control Register
GTUDDTYC	: General PWM Timer Count Direction and Duty Setting Register
GTIOR	: General PWM Timer I/O Control Register
GTINTAD	: General PWM Timer Interrupt Output Setting Register
GTST	: General PWM Timer Status Register
GTBER	: General PWM Timer Buffer Enable Register
GTITC	: General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register
GTCNT	: General PWM Timer Counter
GTCCRA	: General PWM Timer Compare Capture Register A
GTCCRB	: General PWM Timer Compare Capture Register B
GTCCRC	: General PWM Timer Compare Capture Register C
GTCCRD	: General PWM Timer Compare Capture Register D
GTCCRE	: General PWM Timer Compare Capture Register E
GTCCRF	: General PWM Timer Compare Capture Register F
GTPR	: General PWM Timer Cycle Setting Register
GTPBR	: General PWM Timer Cycle Setting Buffer Register
GTPDBR	: General PWM Timer Cycle Setting Double-Buffer Register
GTADTRA	: General PWM Timer A/D Converter Start Request Timing Register A
GTADTBRA	: General PWM Timer A/D Converter Start Request Timing Buffer Register A
GTADTDBRA	: General PWM Timer A/D Converter Start Request Timing Double-Buffer Register A
GTADTRB	: General PWM Timer A/D Converter Start Request Timing Register B
GTADTBRB	: General PWM Timer A/D Converter Start Request Timing Buffer Register B
GTADTDBRB	: General PWM Timer A/D Converter Start Request Timing Double-Buffer Register B
GTDTCR	: General PWM Timer Dead Time Control Register
GTDVU	: General PWM Timer Dead Time Value Register U
GTDVD	: General PWM Timer Dead Time Value Register D
GTDBU	: General PWM Timer Dead Time Buffer Register U
GTDBD	: General PWM Timer Dead Time Buffer Register D
GTSOS	: General PWM Timer Output Protection Function Status Register
GTSOTR	: General PWM Timer Output Protection Function Temporary Release Register
OPSCR	: Output Phase Switching Control Register

source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 2

Some registers outside GPT must be configured first:

- PWPR must be set to 0 and then to 0x40 to write-enable the register P107PFS
  (PWPR is a byte-wide register at 0x4004085C).
- P107PFS must have its field PMR set to 1 and its field PSEL set to 00011b to enable the output signal GTIOCA to be available on P107. Hence, P107 is no longer a GPIO pin but it became a pin connected to the GPT channel 8 peripheral.
  (P107PFS is a word-wide register at 0x4004085C).
- bit-6 of MSTPCRD must be reset to 0 to enable GPT channel 8, otherwise it remains in low power state, hence, not operational
  (MSTPCRD is a word-wide register at 0x40047008);

source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 2

GTWP - General PWM Timer Write-Protection Register

Most registers of the GPT are protected against accidental modification, these can only be written to after write-enabled by GTWP. After reset the registers are write-enabled.

To write-enable, GTWP must be written with (`0xA5 << 8 | 0`)

The affected registers are: GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTIBCSR, GTCR, GTUDDTYC, GTIOR, GTINTAD,GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR

Since the default value of GTWP is write-enable, there is no need to change this register.

source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 2

GTSTR - General PWM Timer Software Start Register

One bit for each channel.

Write 1 to start that channel.

Write 0 has no effect.

Bit i controls channel i

A channel may be started by GTCR as well.

source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 2

GTUDDTYC - General PWM Timer Count Direction and Duty Setting Register

bit 0 - UD - set to count UP

bits 17,16 - OADTY - 00 = GTIOCA duty cycle depends on compare match

other bits must remain 0

GTUDDTYC is a word-wide register at 0x40078830.

source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 2

GTIOR - General PWM Timer I/O Control Register

bits 4..0 - 11001b - Initial output is high, low output at GTCCRA compare match,
high output at cycle end.

bit 8 - OAE - set to 1 to enable the GTIOCA pin output

other bits must remain at 0.

GTIOR is a word-wide register at 0x40078834.

source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 2

GTCCRA - General PWM Timer Compare Capture Register A

Holds the number of PCLKD ticks at the moment when the PWM signal changes to low, this is, after 25% of the cycle, considering that the cycle starts at high (configured in GTIOR) and remains high for the first 25% of the cycle.

When PCLKD is configured for 120 MHz, and the desired PWM cycle is 10 ms, 25% corresponds to 7.5ms. It is required 300,000 PCLKD cycles for the high time and 1,200,000 PCLKD cycles for the PWM cycle. Since the counting starts at zero, the actual value programmed to GTCCRA is 299,999 (or 0x493DF).

GTCCRA is a word-wide register at 0x4007884C.

source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 2

GTPR - General PWM Timer Cycle Setting Register

Considering the calculation presented for GTCCRA, GTPR must be configured with the value 1.200,000 -1 (or 0x124F7F).

GTPR is a word-wide register at 0x40078864.

source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 2

GTCR - General PWM Timer Control Register

Bits 0 - CST - 1 means count in progress

Bits 18..16 - MD - 000 means saw-wave PWM

Bits 26..24 - TPCS - Timer Prescaler - 000 means PCLKD/1

GTCR is a word-wide register at 0x4007882C.

source: Renesas S7 Series Microcontrollers User's Manual

LAB4 – ACTIVITY 3

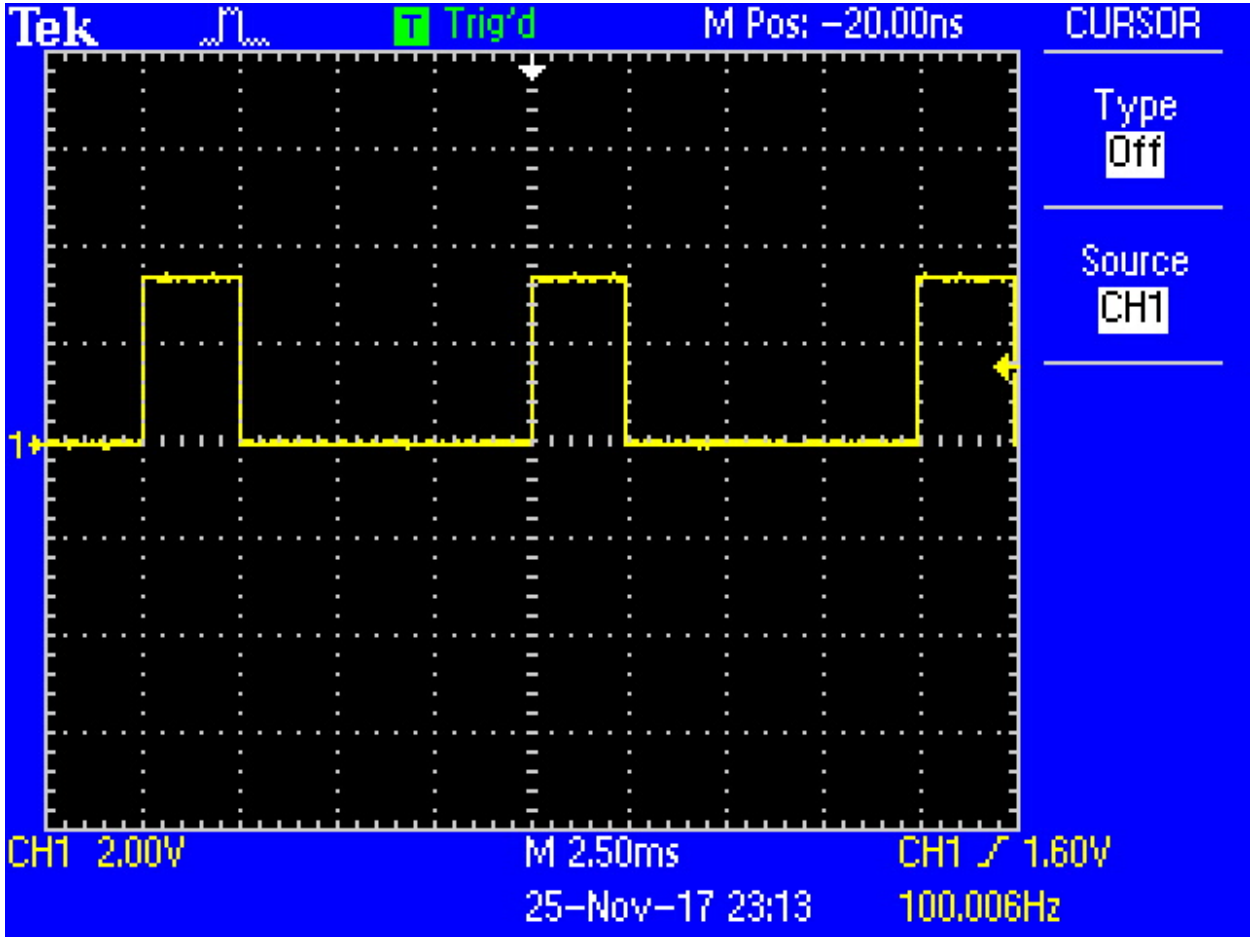
Algorithm

1. Program PWPR to write-enable P107PFS. Write 0 then 0x40 to PWPR.
2. Program P107PFS to put P107 into GTIOCA mode. PSEL = 3, PMR =1
3. Program MSTPCRD bit 6 to enable the power to GPT channel 8. MSTPD6 = 0.
4. Program GTUDDTYC so that the timer counts up and GTIOCA duty cycle depends on compare match to GTCCRA. GTUDDTYC = 1.
5. Program GTIOR so that the cycle starts high and changes to low when a match to GTCCRA occurs. Also, enable GTIOCA output. GTIOR = 0x119.
6. Program GTCCRA to 25% of the cycle (300,000 -1).
7. Program GTPR to the cycle period (1,200,000-1).
8. Start the timer in saw-wave mode with PCLKD/1.

LAB4 – ACTIVITY 4

Verify the operation of the PWM.

Connect a scope to pin P107 (labeled P17 on the board) and verify that a 100 Hz rectangular waveform with a 25% duty cycle is present.



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