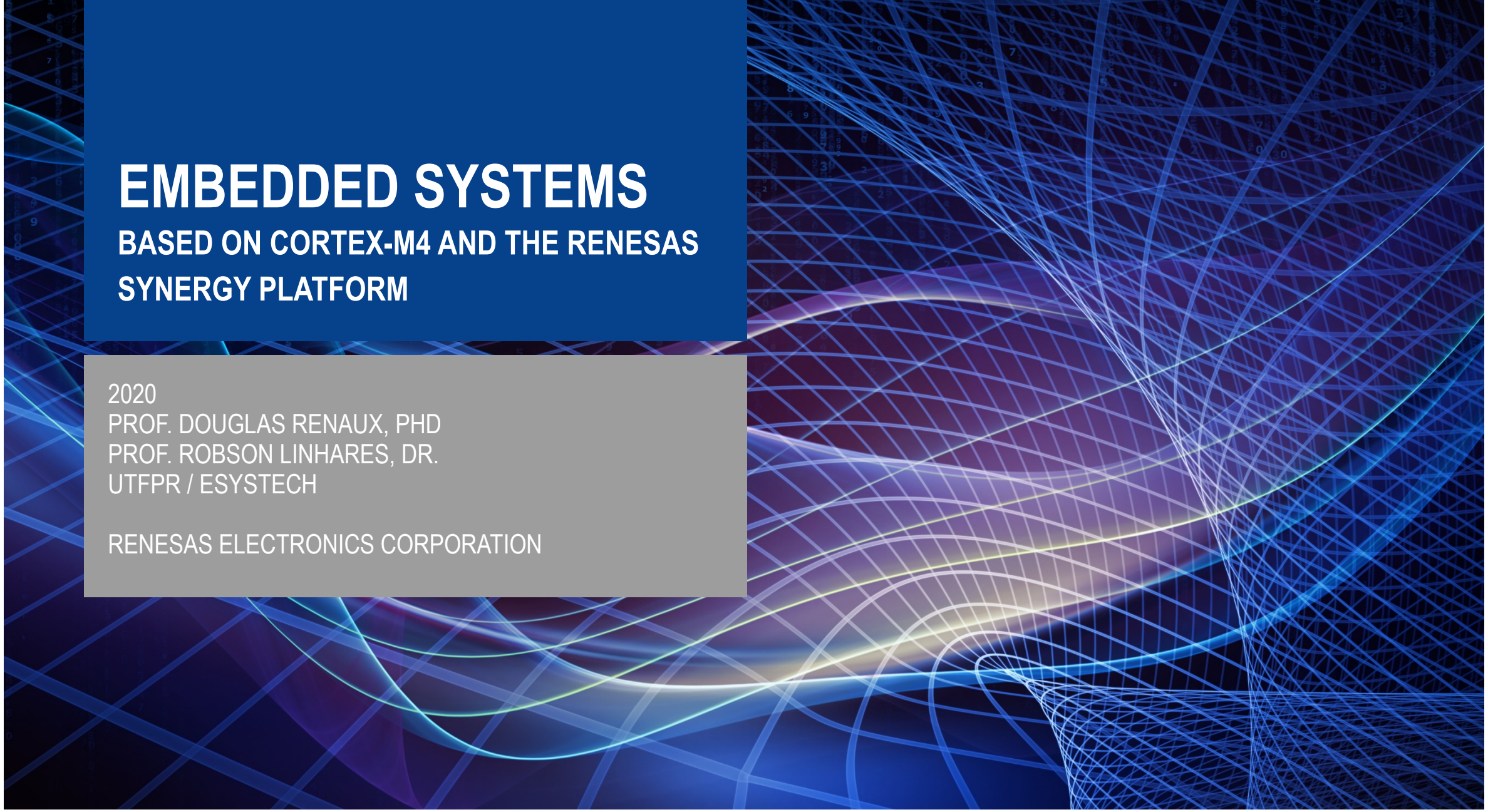

EMBEDDED SYSTEMS

BASED ON CORTEX-M4 AND THE RENESAS SYNERGY PLATFORM

2020
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4 – MEMORY

- Introduction
- Non-Volatile Memory
- Static RAM
- Dynamic RAM

MEMORY – INTRODUCTION

Semiconductor Memory

- Electronic components that store information.
- Memory is an essential part of a microprocessor-based system.

MEMORY – INTRODUCTION

Types of Memory devices:

- **Volatile:** memory devices that do not retain information when power is removed.
  Example: PC main memory
- **Non-volatile:** memory devices that retain information even when not powered.
  Example: flash drive

MEMORY – INTRODUCTION

Types of Volatile Memory:

- **Static:** retain information as long as the device is powered.
- **Dynamic:** do not retain information, even when powered. Hence, dynamic memories do need to be constantly "remembered" of the information they store. This process is called refresh. It must occur every few milliseconds in order not to loose information.

TYPES OF NON-VOLATILE MEMORY

Some of the types of non-volatile memory are:

- ROM: (or masked ROM) - Read Only Memory,
- EPROM: Erasable Programmable Read Only Memory,
- EEPROM: Electrically Erasable Programmable Read Only Memory,
- NOR Flash,
- NAND Flash,
- FeRAM: Ferro Electric Random Access Memory.

TYPES OF VOLATILE MEMORY

Some of the types of volatile memory are:

- SRAM: Static Random Access Memory
- DRAM: Dynamic Random Access Memory
- DDR: Double Data Rate

MEMORY – CONCEPT

A memory device behaves like an array in C.

The memory device that is pictured here has size 2^{20} and every addressable location can store 8 bits. The three control lines indicate when the memory is being addressed, if it is being read or written.

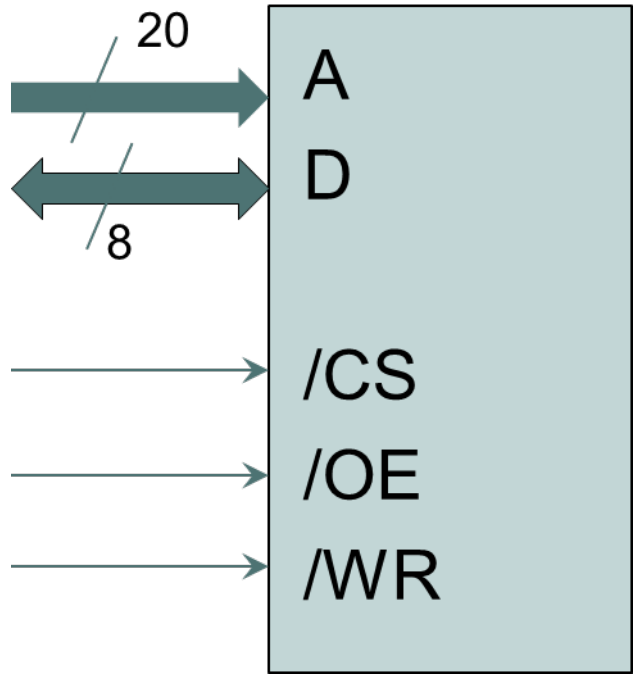
A – address bus. Input. With N address lines it is possible to index 2^N unique locations.

D – data bus. Bidirectional. Width corresponds to the number of bits stored in each addressable location.

/CS – active low chip select. When active, this device is selected.

/OE – active low output enable. When active, indicates the device is being read.

/WR – active low write. When active, indicates the device is being written to.

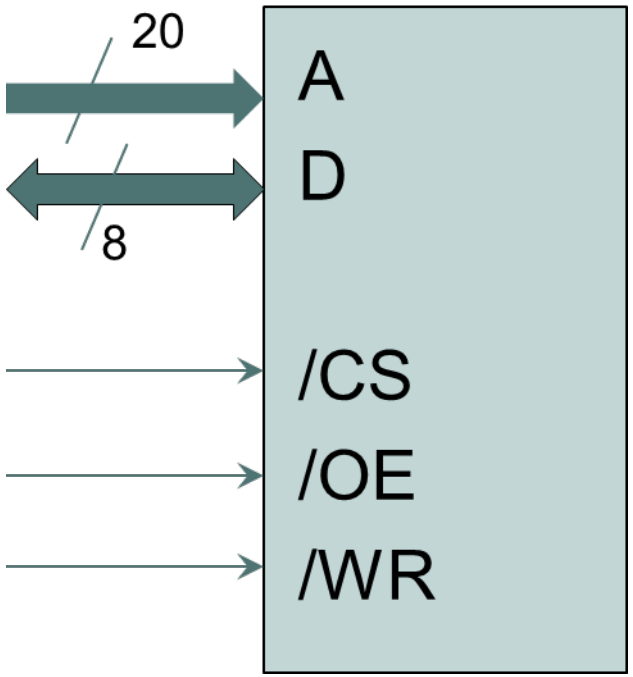


source: Authors

MEMORY – CONCEPT

A memory device behaves like an array in C

Physical view

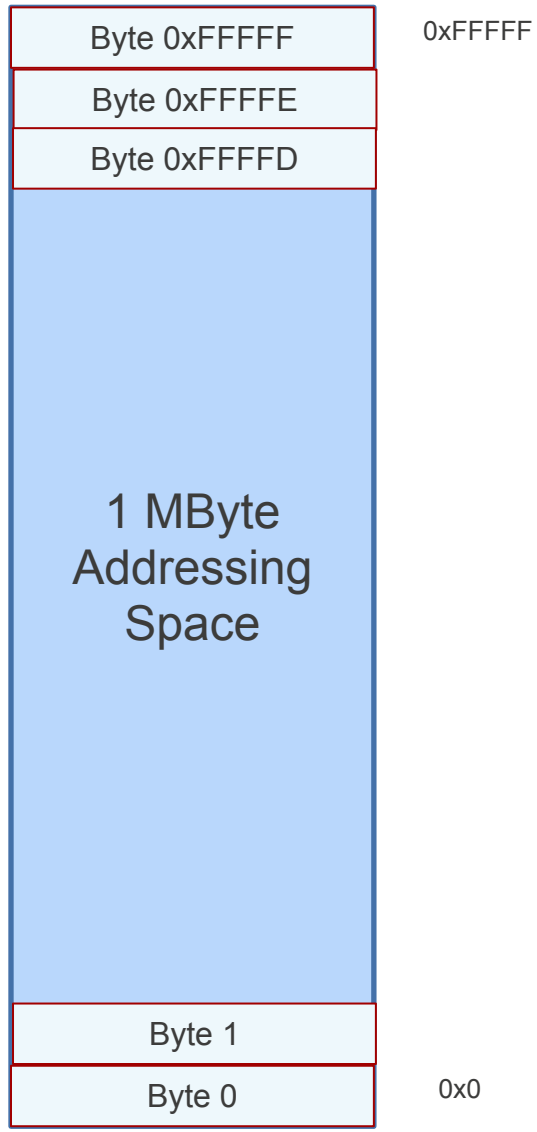


2^{20} = 1,048,576
= 1 Mega
addressable locations

each location holds 8 bits

hence, total storage is 1 Mbyte corresponding to a vector of 1,048,576 8-bit cells

Logical view

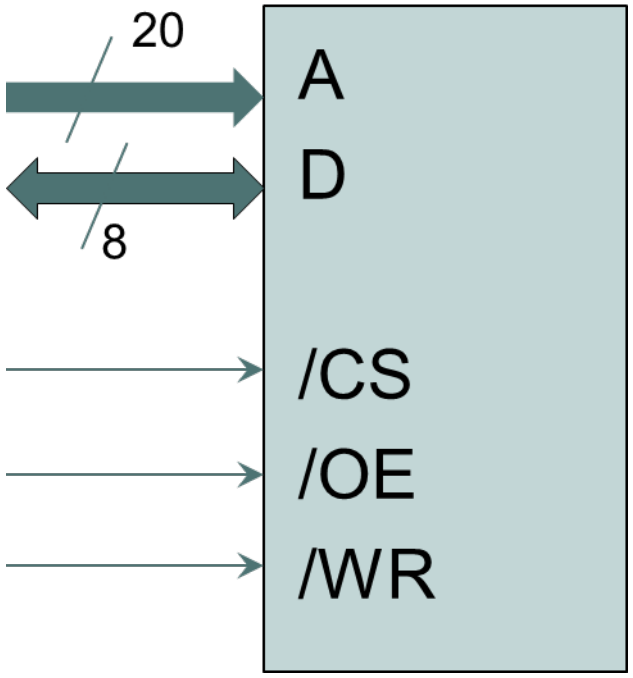


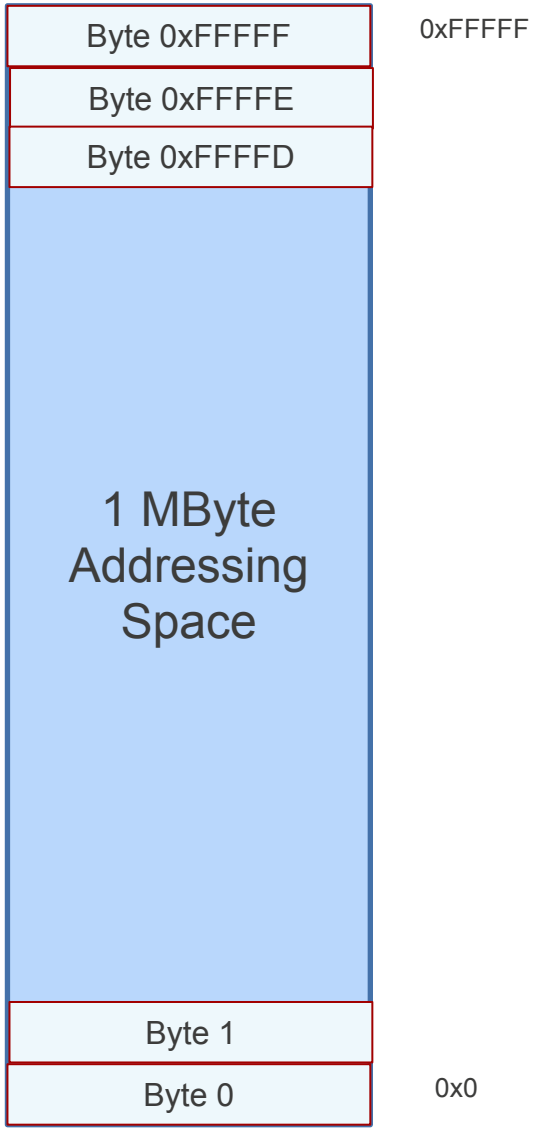
source: Authors

MEMORY – CONCEPT

From an external perspective, e.g. the perspective of the processor.
This device is an array of 2^{20} locations of 8 bits each.
Hence, the size of the memory is 1 MByte (1,048,576) and the width is 8 bits. Or, 1 M x 8 bits resulting in 8 Mbits of total storage capacity.

Internally the organization is different. Possibly this memory is organized as a matrix of 1024 line and 1024 columns with 8 bits in each position. Resulting in the capacity of 1024 x 1024 x 8 = 8 Mbits.





source: Authors

SAMPLE PROBLEM

Assume the only memory chip available is 1 M x 8 bits. How to implement 2M x 32bits = 8 MBytes of memory to a Cortex-M4 with data bus width of 32-bits?

Memory should be located from address 0x1000 0000 on.

SAMPLE PROBLEM

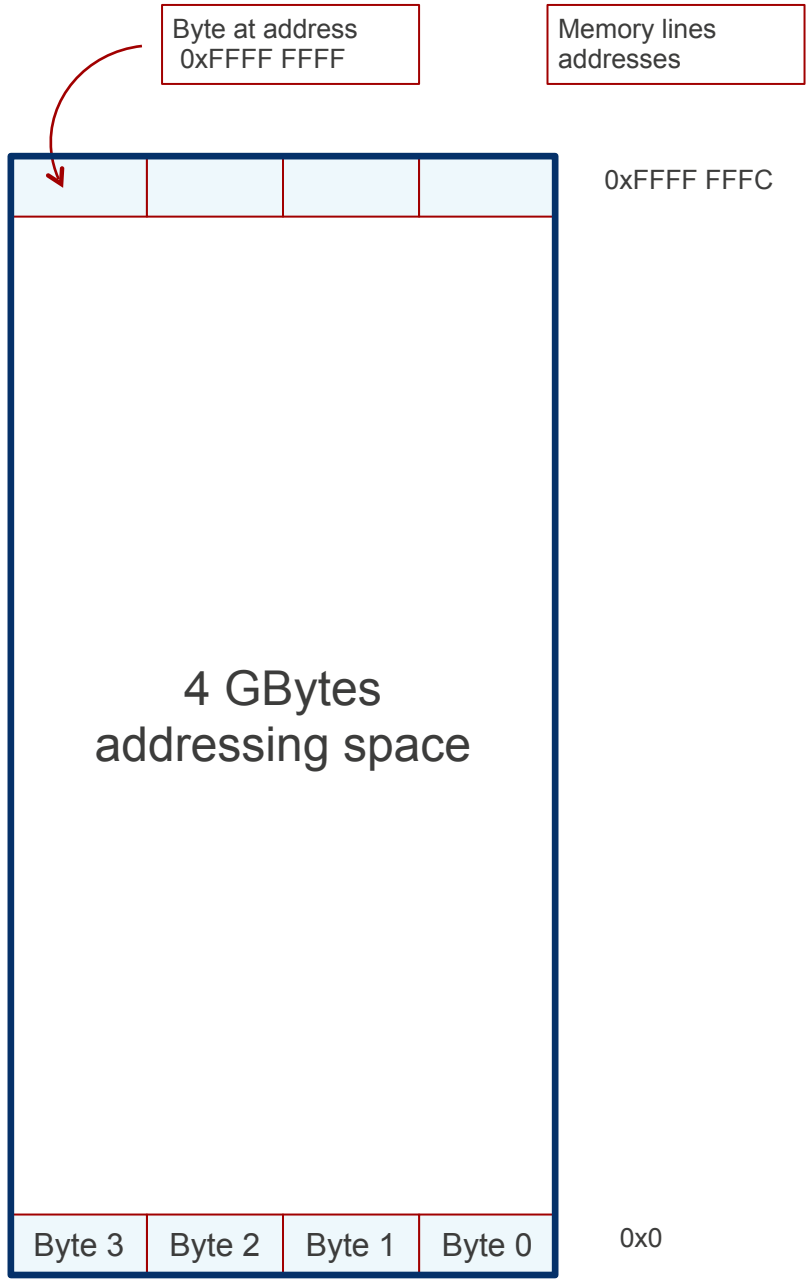
The addressing space of a Cortex-M is 4 GBytes, i.e. 2^{32} = 4,294,967,296.

If physical memory is 32-bit wide (4 bytes) then there are 1 G lines (1,073,741,824). Each of these lines is addressable by its LSByte address.

Hence, 30 address lines are required to select a single memory line (as 2^{30} = 1 G)

The address lines A31-A2 are used to select on of the 1G lines while address lines A1 and A0 are used to select a byte in the memory line

Memory address lines have their A1-A0 addresses set to 0. Hence, the first memory line is at address 0x0000 0000, the second at address 0x0000 0004 and so on.



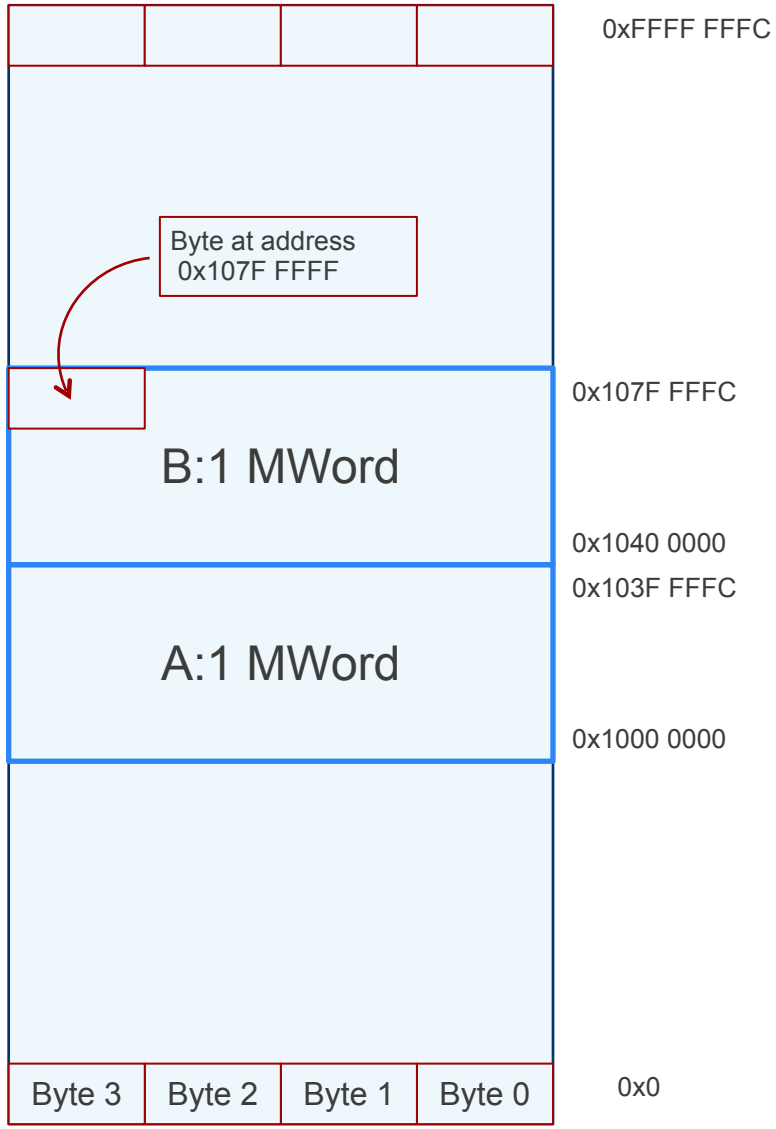
source: Authors

SAMPLE PROBLEM

Since the capacity of each chips is 1 Mbit and 8 Mbits are required, 8 chips must be used.

Since the processor data bus is 32-bit wide and the memory is 8-bit wide, 4 chips are put side-by-side to complete one 32-bit wide memory line.

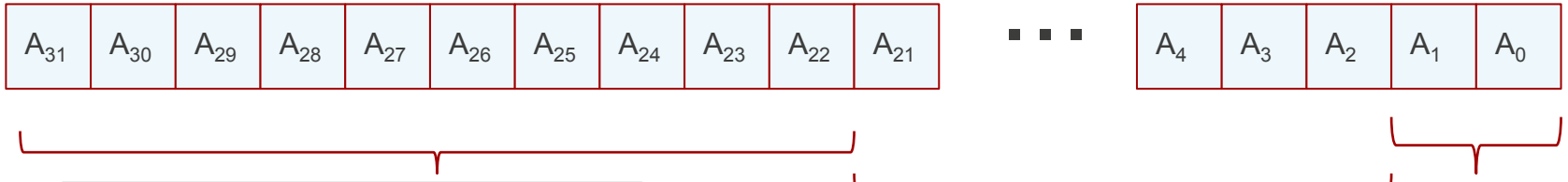
The first set of 4 chips have a combined capacity of 8 MWords and are mapped from address 0x1000 0000 to 0x103F FFFF.
The second set of 4 chips are mapped from 0x1040 0000 to 0x107F FFFF.



source: Authors

SAMPLE PROBLEM

Selecting the address lines for CS (Chip Select) and for memory line addressing. These are the 32-bit addresses from the Cortex-M processor:



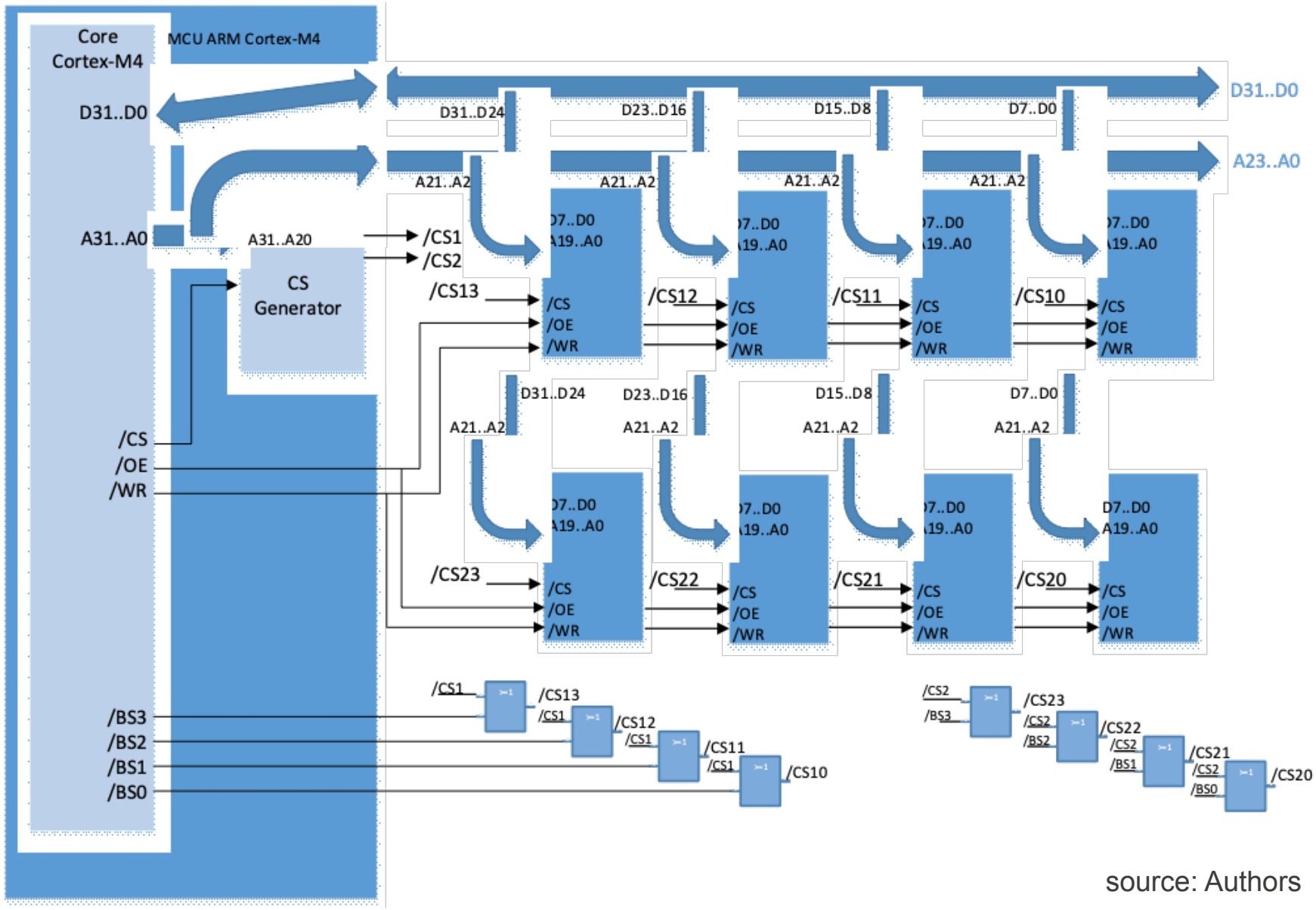
these 10 address lines identify each of the 1 MWord regions.

In region A these address lines must be at 0001 0000 00 b (0x100)
While for region B:
0001 0000 01 b (0x104)
(these addresses are constant inside each of the 1MWord regions)

these 20 lines select one of the 1 G memory lines

these address lines select the byte in the memory line

source: Authors



/CS1 must be active in the range 0x1000 0000 to 0x103F FFFF

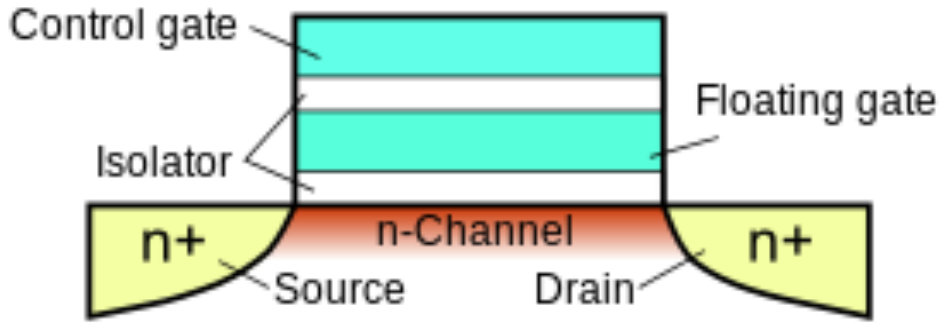
/CS2 must be active in the range 0x1040 0000 to 0x107F FFFF

source: Authors

NOR FLASH MEMORY

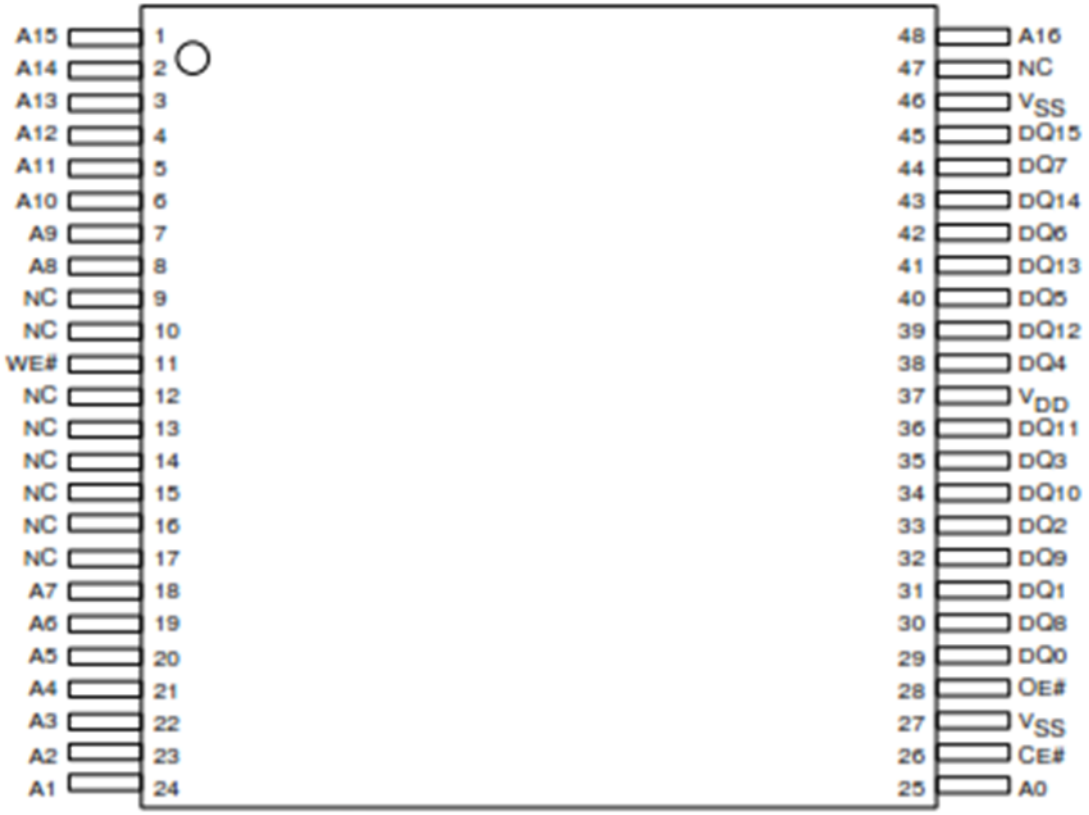
NOR Flash memory is frequently used in embedded systems to store non-volatile data, particularly code and constants.

Each bit of a NOR Flash memory is implemented by a single floating gate MOS. The floating gate may be charged and, since the floating gate is isolated, the charges are trapped into de gate. Hence, the two possible states are: charges trapped in the floating gate vs no charges trapped in the floating gate.



source: wikimedia.org (CC)

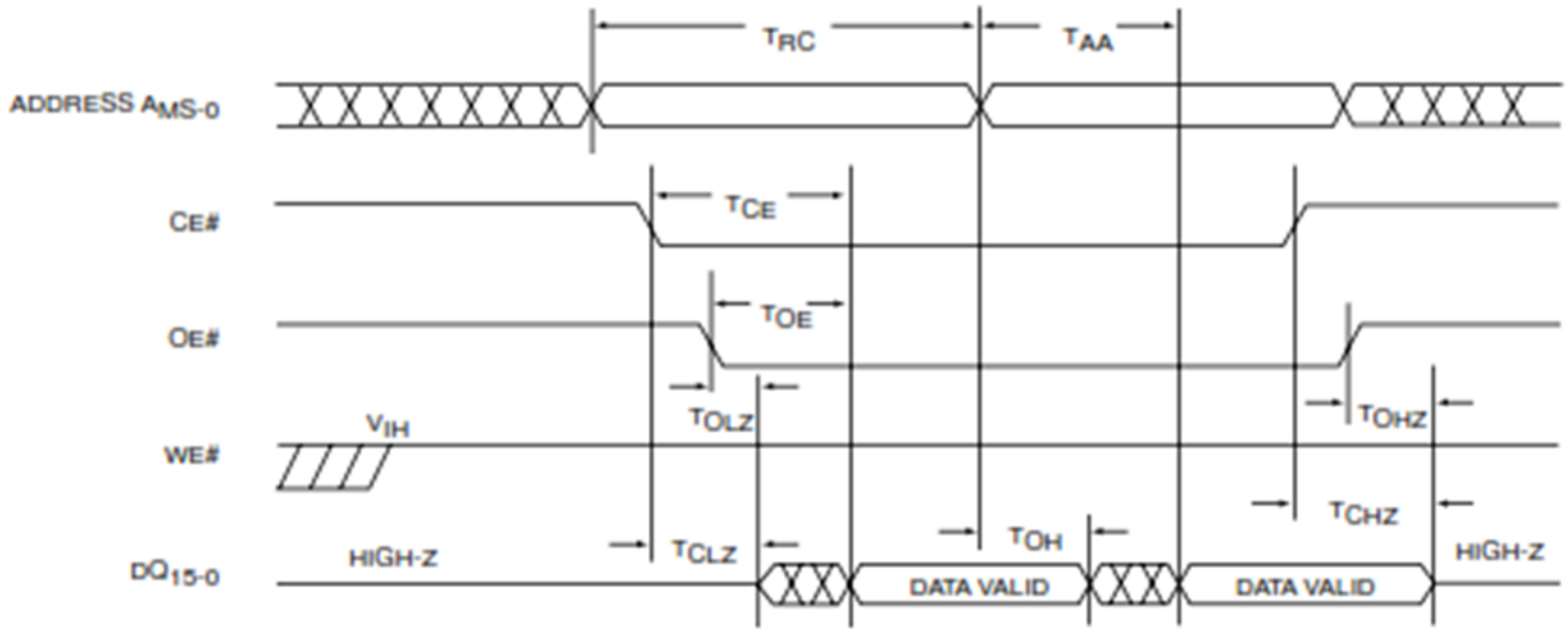
EXAMPLE OF A FLASH MEMORY DEVICE 128K X 16 BITS



Symbol	Pin Name	Functions
A_{16} -A_0	Address Inputs	To provide memory addresses. During Sector-Erase A_{MS}-A_{11} address lines will select the sector. During Block-Erase A_{MS}-A_{15} address lines will select the block.
DQ_{15}-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
V_{DD}	Power Supply	To provide power supply voltage:
V_{SS}	Ground	
NC	No Connection	Unconnected pins.

EXAMPLE OF A FLASH MEMORY DEVICE 128K X 16 BITS

The operation of a NOR Flash memory is straightforward: the processor sets the address to be read, and activates Chip Select (CE#) and Output Enable (OE#) after a delay (TCE of TOE) valid data is presented on the data bus.

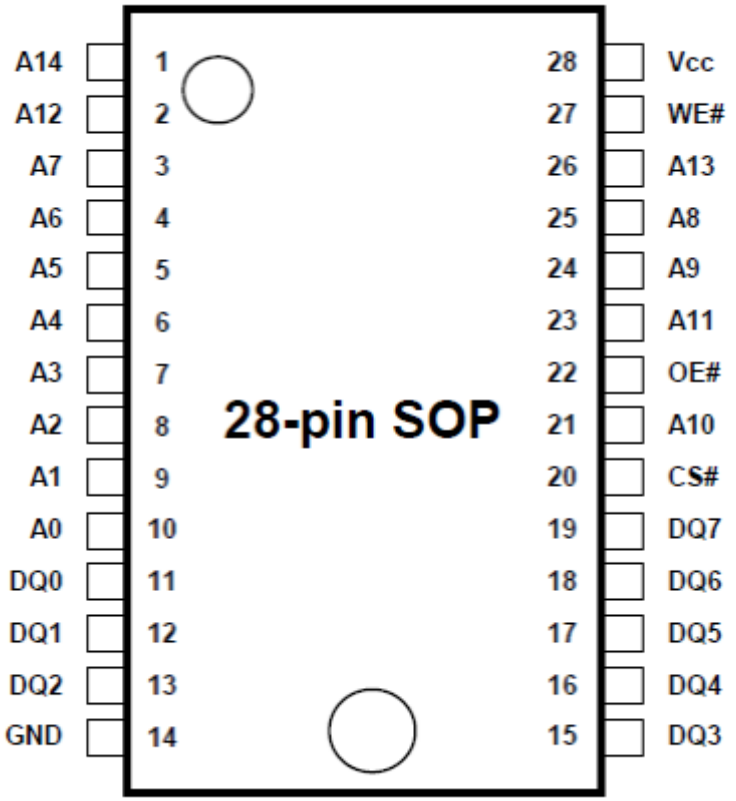


SRAM EXAMPLE

R1LV5256E Series

256Kb Advanced LPSRAM (32k word x 8bit)

Pin name	
Vcc	Power supply
Vss (GND)	Ground
A0 to A14	Address input
DQ0 to DQ7	Data input/output
CS#	Chip select
WE#	Write enable
OE#	Output enable



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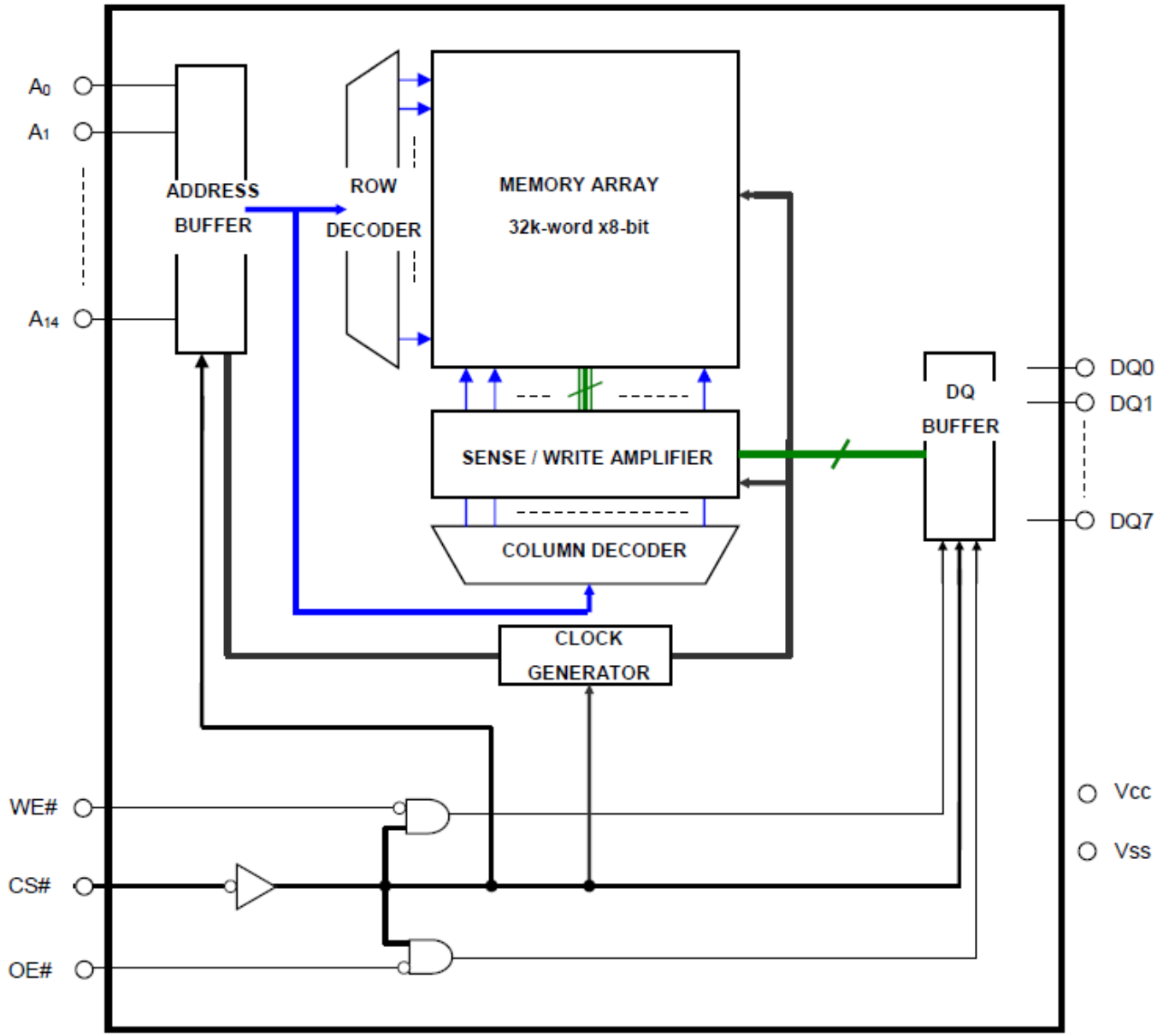
INTERNAL ORGANIZATION



Operation Table

CS#	WE#	OE#	DQ0~7	Operation
H	X	X	High-Z	Stand-by
L	L	X	Din	Write
L	H	L	Dout	Read
L	H	H	High-Z	Output disable

Note 1. H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}

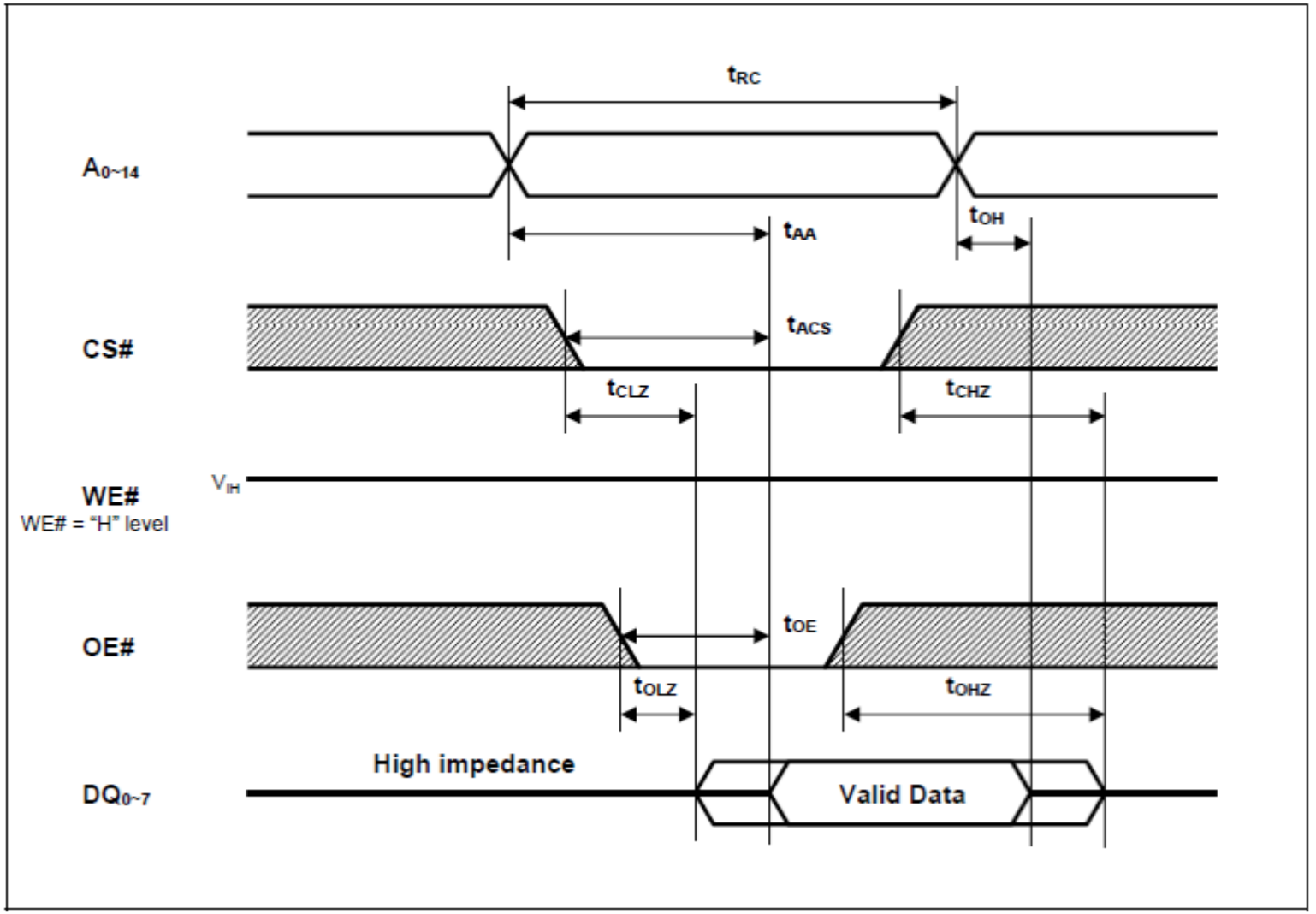
READ CYCLE

Read Cycle timing diagram

Read Cycle

Parameter	Symbol	Min.	Max.
Read cycle time	t_{RC}	55	-
Address access time	t_{AA}	-	55
Chip select access time	t_{ACS}	-	55
Output enable to output valid	t_{OE}	-	30
Output hold from address change	t_{OH}	10	-
Chip select to output in low-Z	t_{CLZ}	5	-
Output enable to output in low-Z	t_{OLZ}	5	-
Chip deselect to output in high-Z	t_{CHZ}	0	20
Output disable to output in high-Z	t_{OHZ}	0	20

Read Cycle



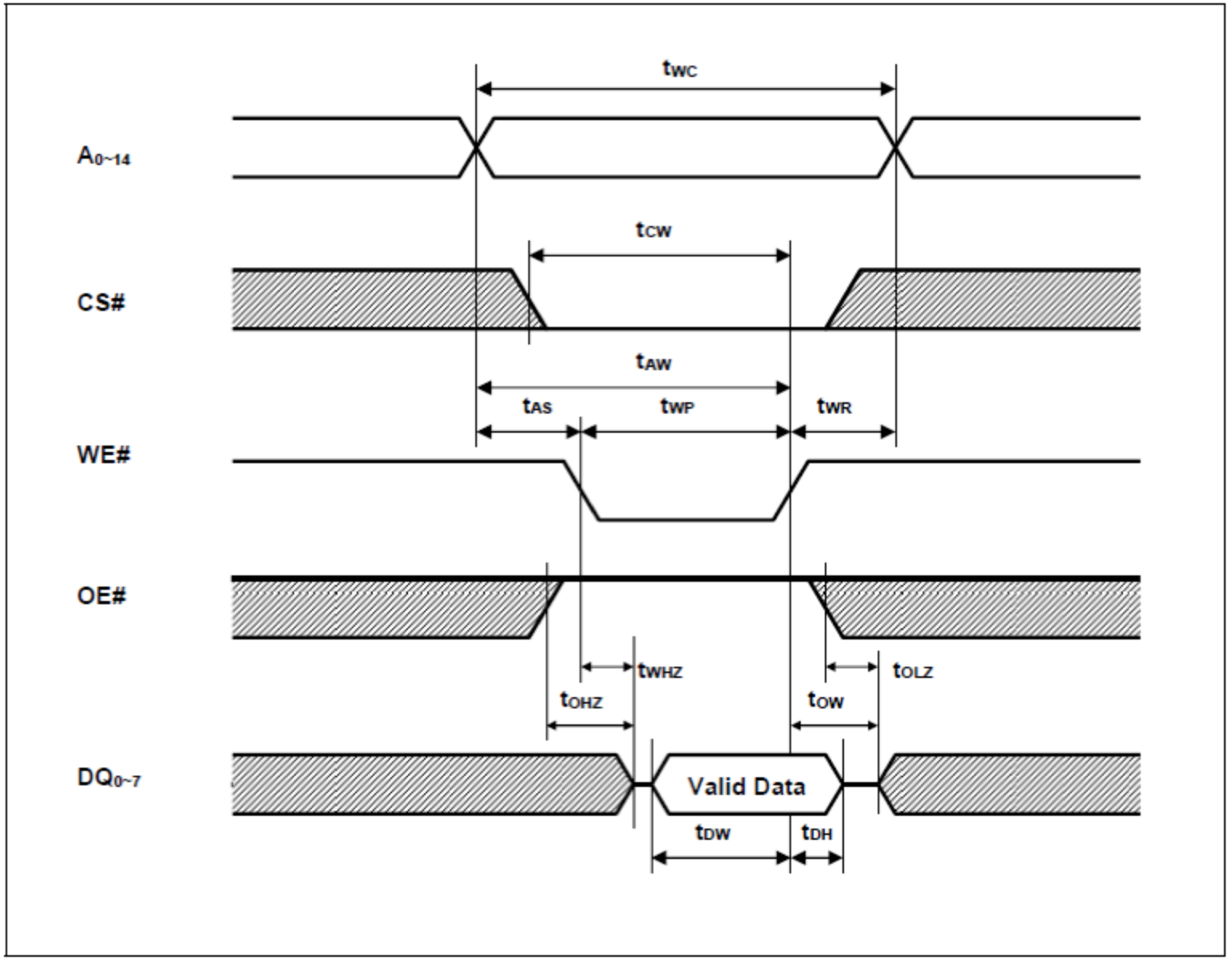
WRITE CYCLE

Write Cycle timing diagram

Write Cycle

Parameter	Symbol	Min.	Max.
Write cycle time	t_{WC}	55	-
Address valid to end of write	t_{AW}	50	-
Chip select to end of write	t_{CW}	50	-
Write pulse width	t_{WP}	40	-
Address setup time	t_{AS}	0	-
Write recovery time	t_{WR}	0	-
Data to write time overlap	t_{DW}	25	-
Data hold from write time	t_{DH}	0	-
Output enable from end of write	t_{OW}	5	-
Output disable to output in high-Z	t_{OHZ}	0	20
Write to output in high-Z	t_{WHZ}	0	20

Write Cycle (1) (WE# CLOCK)

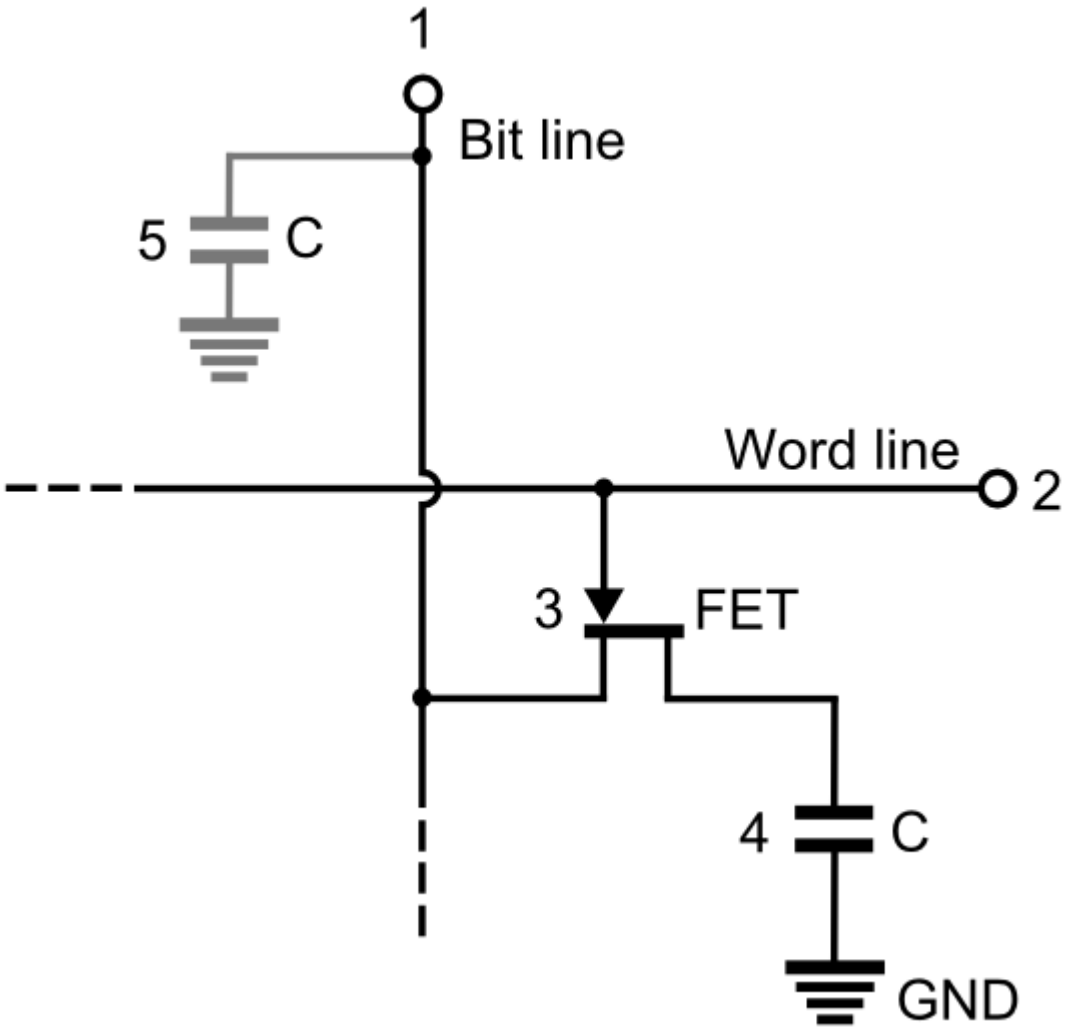


DYNAMIC RAM

In a dynamic RAM, each bit is implemented by a circuit consisting of a capacitor and a transistor.
The capacitor stores de information (charged vs discharged) and the transistor acts as a switch that connects the capacitor to the Bit Line when that particular bit is accessed.

Because the capacitance is very small and because of leakage, the charge of the capacitor only holds reliably for a few milliseconds, hence, this memory bit must be constantly refreshed.

Also, every read of a memory cell is destructive, hence, after a read the value must be rewritten.



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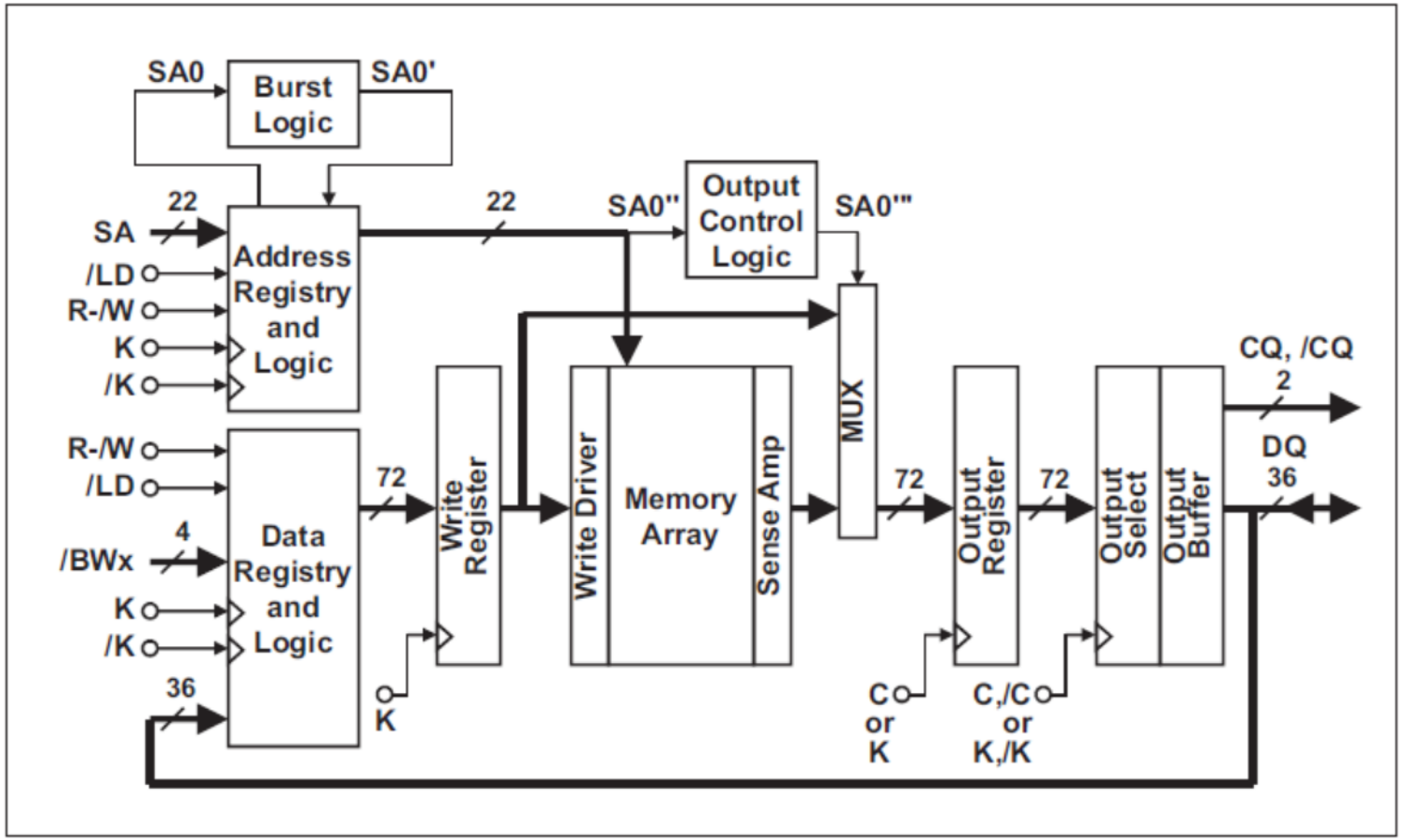
DDR – DOUBLE DATA RATE

[R1Q4A4436RBG]



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