EMBEDDED SYSTEMS

BASED ON CORTEX-M4 AND THE RENESAS SYNERGY PLATFORM

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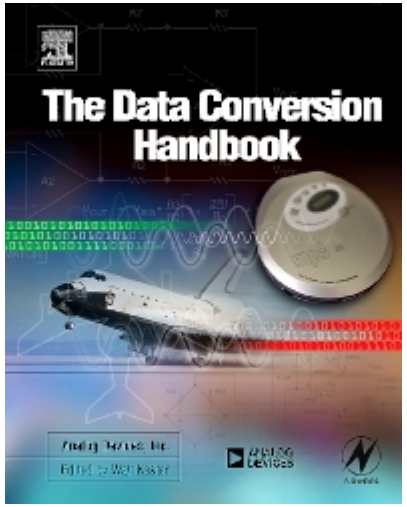
7 – ANALOG INTERFACING

- ADC – Analog to Digital Converter
- DAC – Digital to Analog Converter



recommended readings:
1- http://www.analog.com/en/analog-dialogue/articles/the-right-adc-architecture.html
2- The Data Conversion Handbook, Edited by Walt Kester, Analog Devices Inc.

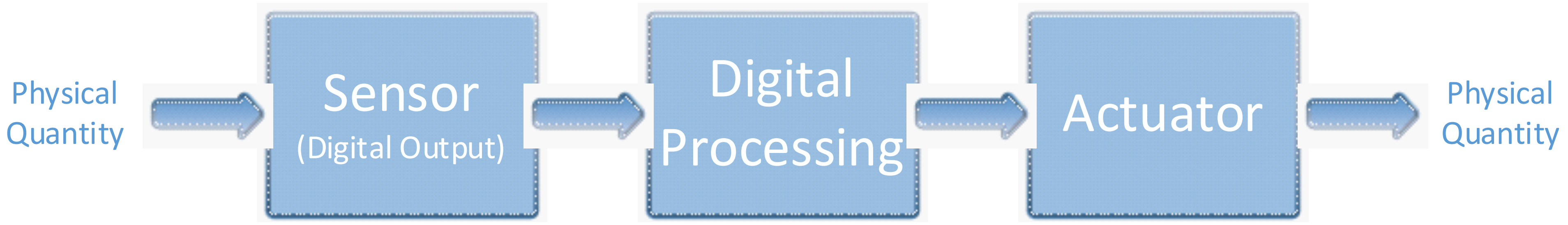
ANALOG VS DIGITAL

- Real world phenomena, such as audio, images, temperature, forces, pressure, and so, can be represented by waveforms that are continuous both in time and amplitude with an infinite resolution.
- Sensors are able to convert these physical quantities into analog electrical signals that can be processed by analog circuits. This was the most common case a few decades ago: radio, audio amplifiers, television, ...
- Nowadays, these physical quantities are converted to a sequence of numbers, i.e. they were digitized, so that they can be processed by a computer (digital processor).

ANALOG VS DIGITAL

Analog	Digital
Physical quantities are converted to electrical signals that are **continuous** both in time and amplitude.	Physical quantities are converted into numeric codes after being **discretized** both in the time (**sampling**) and in amplitude (**quantization**).
Analog signal are prone to **noise** and **distortion** during processing and transmission. Hence, **signal quality decreases** as the signal travels through a system.	Digital signals are much more **robust** to noise and distortion. They can be **restored** to their original value after a noisy system stage.
Analog processing is typically done by a hardwired circuit that performs a **predefined processing** function.	Digital signal processing is typically performed in **software**, thus, its function can be changed **dynamically.**

INTERACTING WITH AN ANALOG WORLD



source: Authors

To interact with the physical quantities in the real world, sensors and actuators are required.

Sensors perceive (“read”) a phenomena and translate it to an electrical signal. The output of a sensor can be an analog signal or a digital signal.

Analog sensors require an Analog-to-Digital conversion before the information is digitally processed.

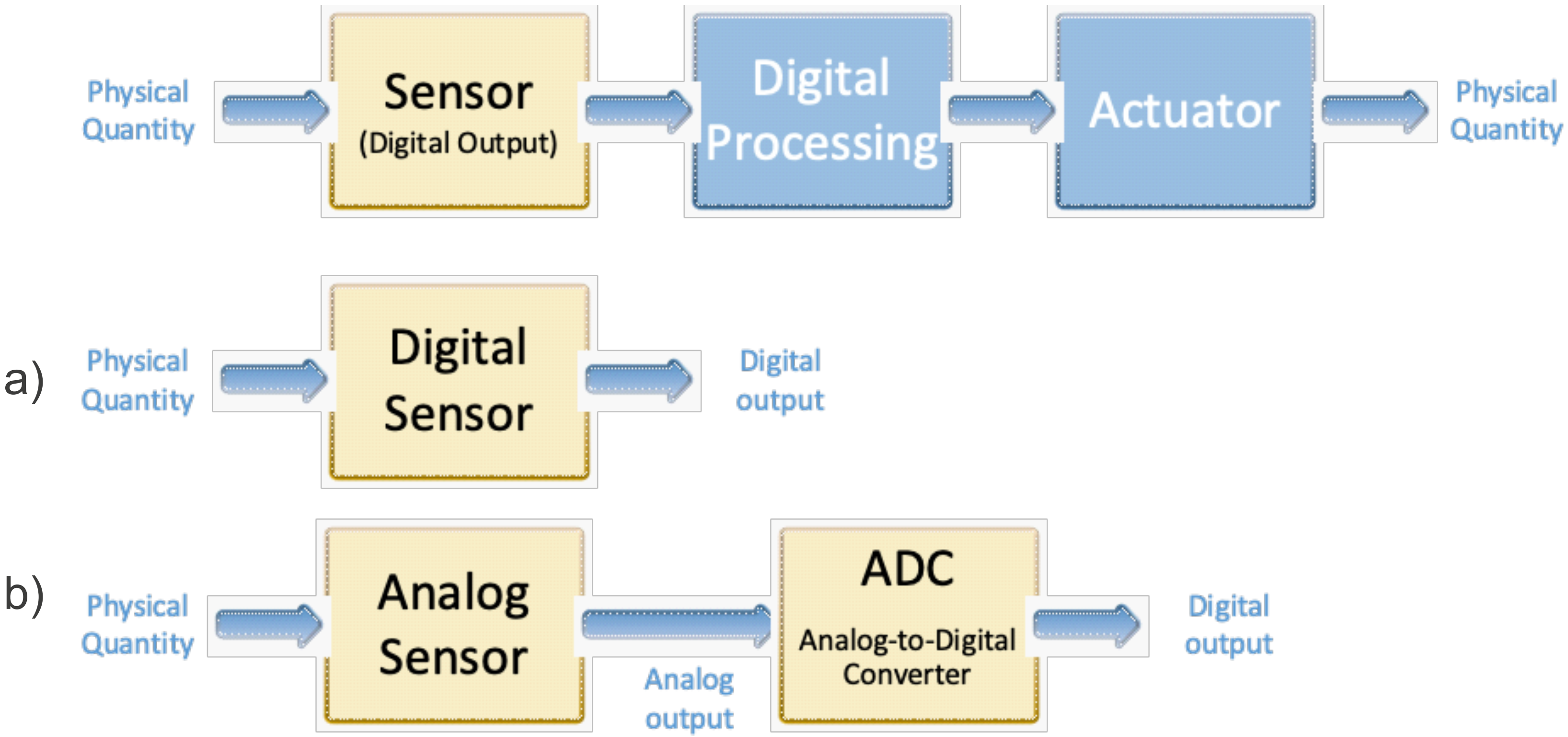
Actuators act upon (“write to”) the environment. The input of an actuator may be an analog or digital signal. To connect a digital processor to an analog actuator a Digital-to-Analog conversion is required.

SENSORS

Two alternatives to the implementation to a sensor in a microprocessed system:

a) Digital Sensor

b) Analog Sensor + ADC



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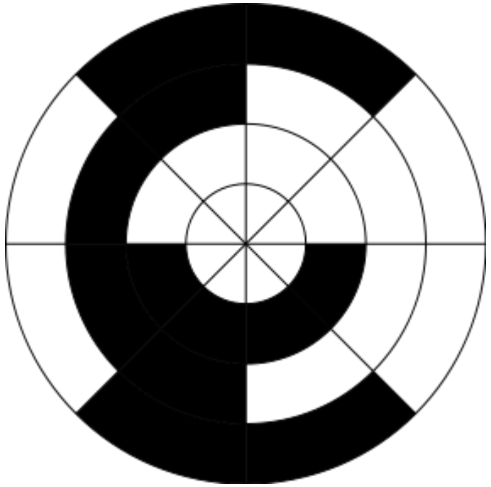
EXAMPLE OF A DIGITAL SENSOR - ENCODER



A rotary optical encoder is an angular position sensor. It consists of a disc with transparent and opaque areas that are detected by a photodetector.

The disc show is of an absolute rotary encoder.

Alternatively, an incremental (or relative) rotary encoder generates pulses to represent angular movement of its axis. A set of two pulse stream, shifted by 90 degrees, allows the detection of the direction of movement in an incremental rotary encoder.

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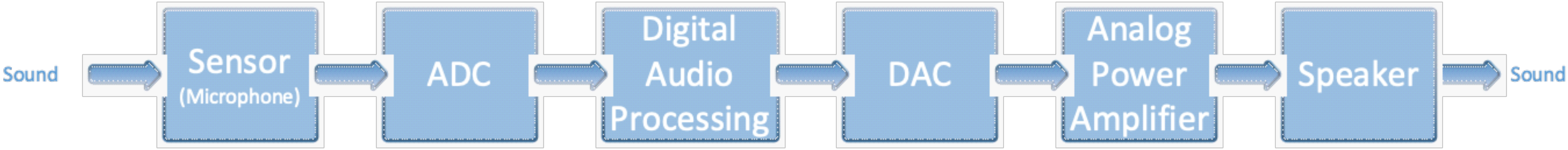
EXAMPLE OF AN AUDIO PROCESSING SYSTEM



source: Authors

In this example, the microphone is an analog sensor;

the speaker is an analog actuator and its driver is the amplifier.

THE ANALOG-TO-DIGITAL CONVERSION PROCESS

The conversion of an analog signal to digital requires several steps:

1. Low-pass filter to guarantee that the input signal spectrum is limited to a given frequency (f_{signal})
2. Sampling (time discretization) - at periodic intervals take samples of the analog signal. The signal amplitude is still an analog value.
3. Quantization (amplitude discretization) - mapping of the continuous amplitude range into a set of discrete values.

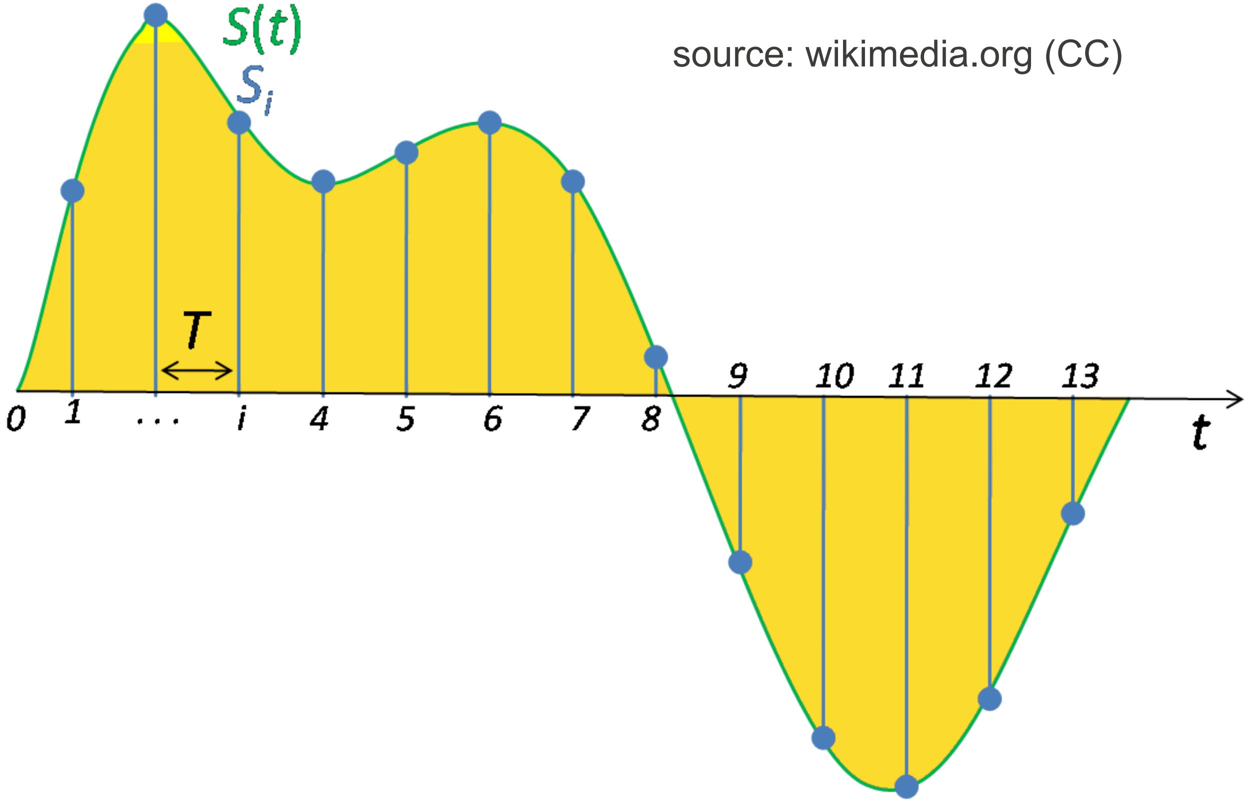
SAMPLING

The green curve represents an analog signal S(t).

This signal is sampled periodically, T being the sampling period, resulting in a discrete sequence of samples Si (i = 1,2,3,...).

The amplitude of each sample is an analog value.

Sampling is performed by a **Sample-and-Hold** (S&H) circuit, represented by a switch and a capacitor. The switch closes momentarily, the capacitor is charged with the current value of the input signal, the switch opens and the value remains "memorized" by the capacitor.



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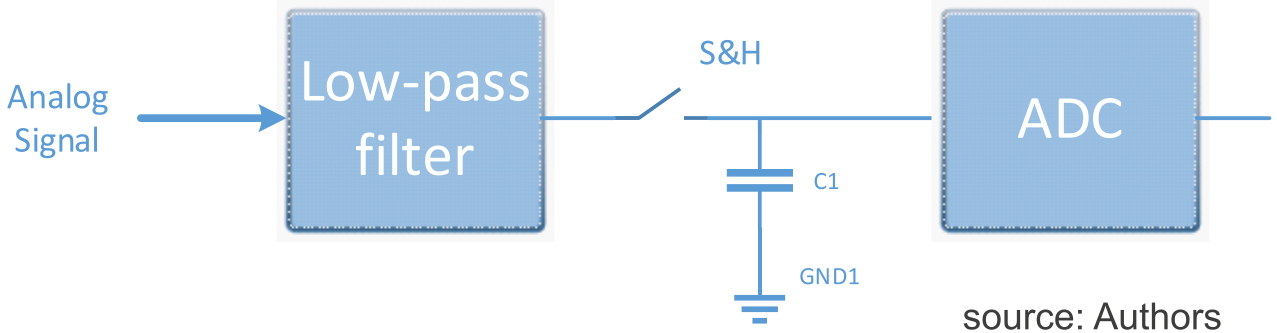

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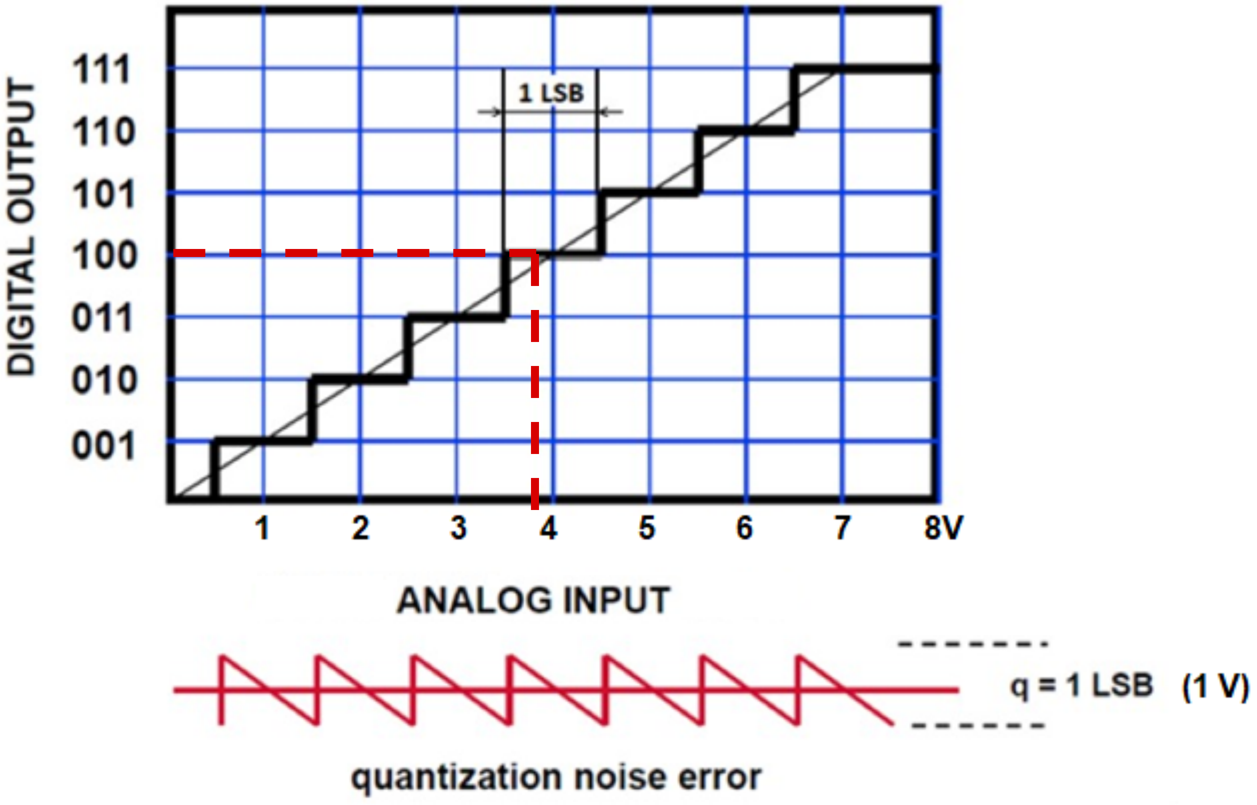
QUANTIZATION

To illustrate de quantization performed by an ADC, consider the transfer function on the right. The horizontal axis is the analog input values to the ADC and the vertical axis are the digital codes produced by the ADC.
In this example the ADC has 3 bits, hence, it is able to represent 8 binary values, from 0 (000) to 7 (111). The input range for this example is from 0 to 8 volts.

The bold line in the graph is the transfer function. If the input voltage is 3.8 volts, the output code will be 4 (100), representing 4 volts. The difference between the actual input value (3.8) and the output value (4) is the quantization error and it is due to the output assuming only a discrete set of values.



source: Renesas DevCon2015
Mitch Ferguson - ADC Specifications

OUTPUT VALUE CALCULATION

a) Unipolar: the quantization levels are distributed from 0 to Vref.

For an ADC with N-bit resolution, there are 2^N quantization levels.

Each quantization level corresponds to an input range q, where

$$q = \frac{Vref}{2^N}$$

Hence, q corresponds to the input range of the LSb (Least Significant bit) of the output code.

The output code (n) of an unipolar ADC, for Vin in the range of 0..(Vref-q) is given by:

$$n = int\left(\frac{Vin}{Vref} * \left(2^N\right) + \frac{1}{2}\right)$$

Example: N = 10 bits, Vref = 5V, Vin = 2.5V

q is 4.88 mV and the output code is 512 (10 0000 0000b)

int(x) results in the integer part of x by truncation.
Hence, for x ≥ 0, int(x) = floor(x)
and for x < 0, int(x) = ceiling(x)

OUTPUT VALUE CALCULATION

b) Bipolar: the quantization levels are distributed from V_{-ref} to V_{+ref}.

Where typically, $V_{-ref} = - V_{+ref}$

Each quantization level corresponds to an input range q, where

$$q = \frac{V_{+ref} - V_{-ref}}{2^N}$$

The output code (n) of a bipolar ADC, for Vin in the range of V_{-ref} .. (V_{+ref} -q) is given by:

$$n = int\left(\frac{Vin - V_{-ref}}{V_{+ref} - V_{-ref}} * \left(2^N\right) + \frac{1}{2}\right)$$

Example: N = 10 bits, V_{+ref} = 5V, V_{-ref} = -5V, Vin = 0V

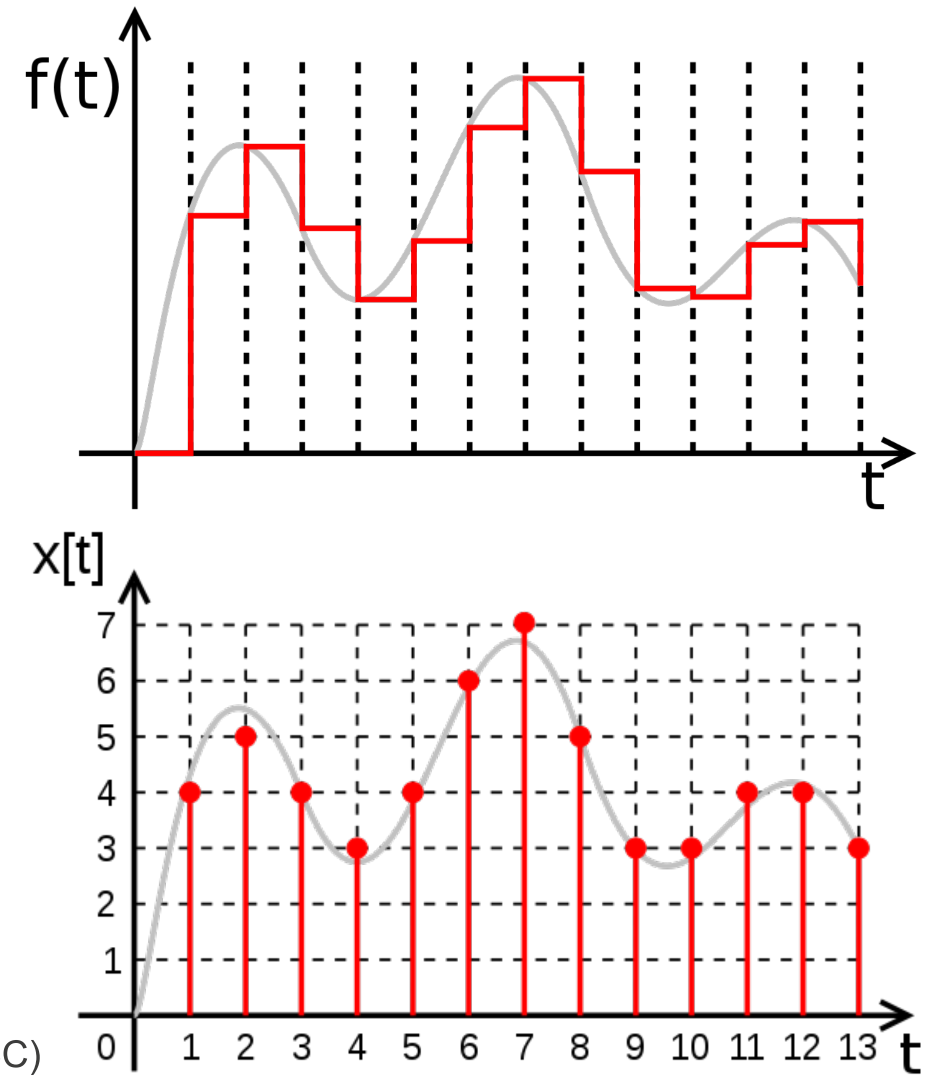
q is 9.76 mV and the output code is 512 (10 0000 0000b)

ANALOG-TO-DIGITAL CONVERSION EXAMPLE

On the upper figure, the grey line represents the input analog signal. The dashed lines indicate the sampling times. The red line is the output of the sample-and-hold. It changes value exactly at the sampling times.

In the lower figure, the red dots represent the output of the ADC. The effect of the quantization error is noticeable as the distance between the red dot and the input signal.

The output of the ADC is the following numeric sequence: 4,5,4,3,4,6,7,5,3,3,4,4,3.



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SIMPLE ADC (3-BIT FLASH)

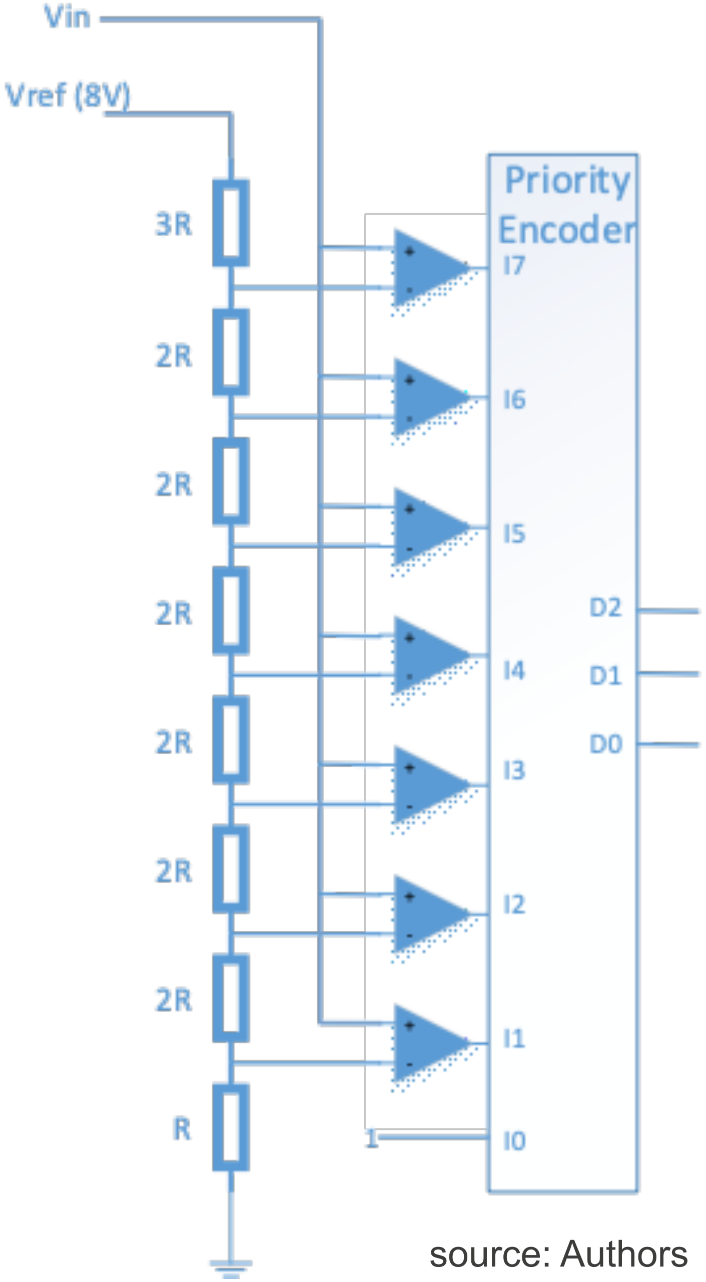
This circuit implements a 3-bit Flash ADC. It is the fastest ADC topology. Vin is in the range 0..Vref and Vref is 8V.

For an ADC with 2N possible output values, 2N -1 comparators are required. Thus, Flash ADCs are usually implemented for a small number of bits.

The resistor ladder provides the appropriate reference voltages for each comparator. In this case: 0.5V, 1.5V, 2.5V, ... 6.5V.

When a comparator detects that the input voltage (Vin) is higher than its reference voltage, its output changes to level 1.

The priority encoder (I7 is highest priority and I0 is lowest) generates the binary code corresponding to the highest priority active input.



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ADC CHARACTERISTICS

Resolution: the number of bits (N) of the output code of the ADC. The number of quantization levels is given by 2^N. A 10-bit ADC has 1024 quantization levels. Hence, for a reference voltage of 1V, each quantization level is 0.97mV (1V/1024). The quantization error is up to ± 0.485mV (.97/2).

Conversion time: how long does it take to the ADC to perform a conversion. Currently, most ADCs integrated in MCUs take from 0.1µs to 1µs. Flash ADCs may take less than 10 ns. The conversion time determines the maximum **sampling frequency** ($f_{sampling}$). By the Nyquist theorem, the sampling frequency should be larger than twice the highest frequency in the input signal, i.e. $f_{sampling} > 2 * f_{signal.}$

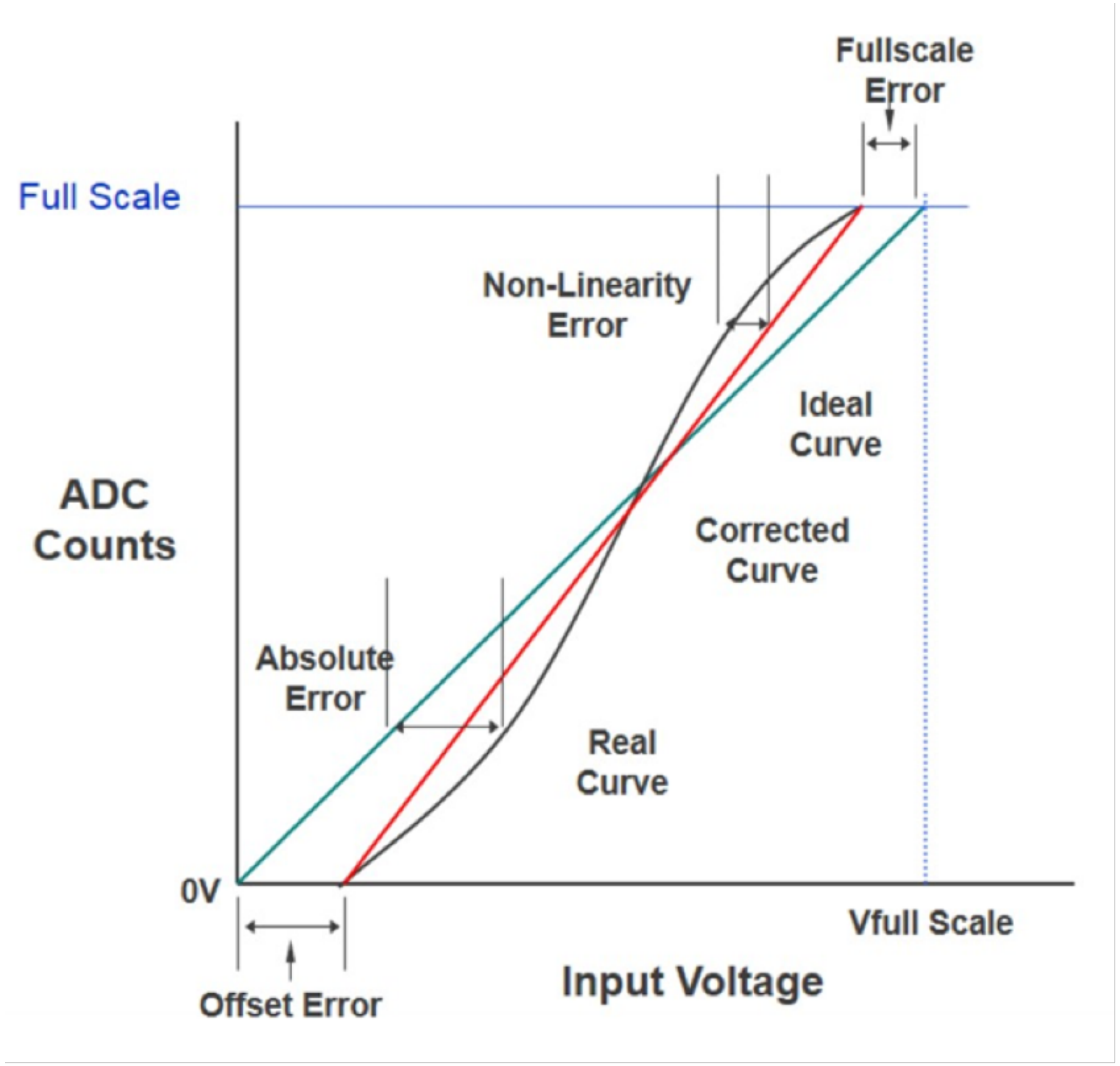
ADC CHARACTERISTICS

DC (and low frequency) errors.

The green line represents the ideal transfer function.

The black line represents the actual transfer function including **offse**t errors and **non-linearity** errors.

The red line corrects non-linearities but offset errors are still present.



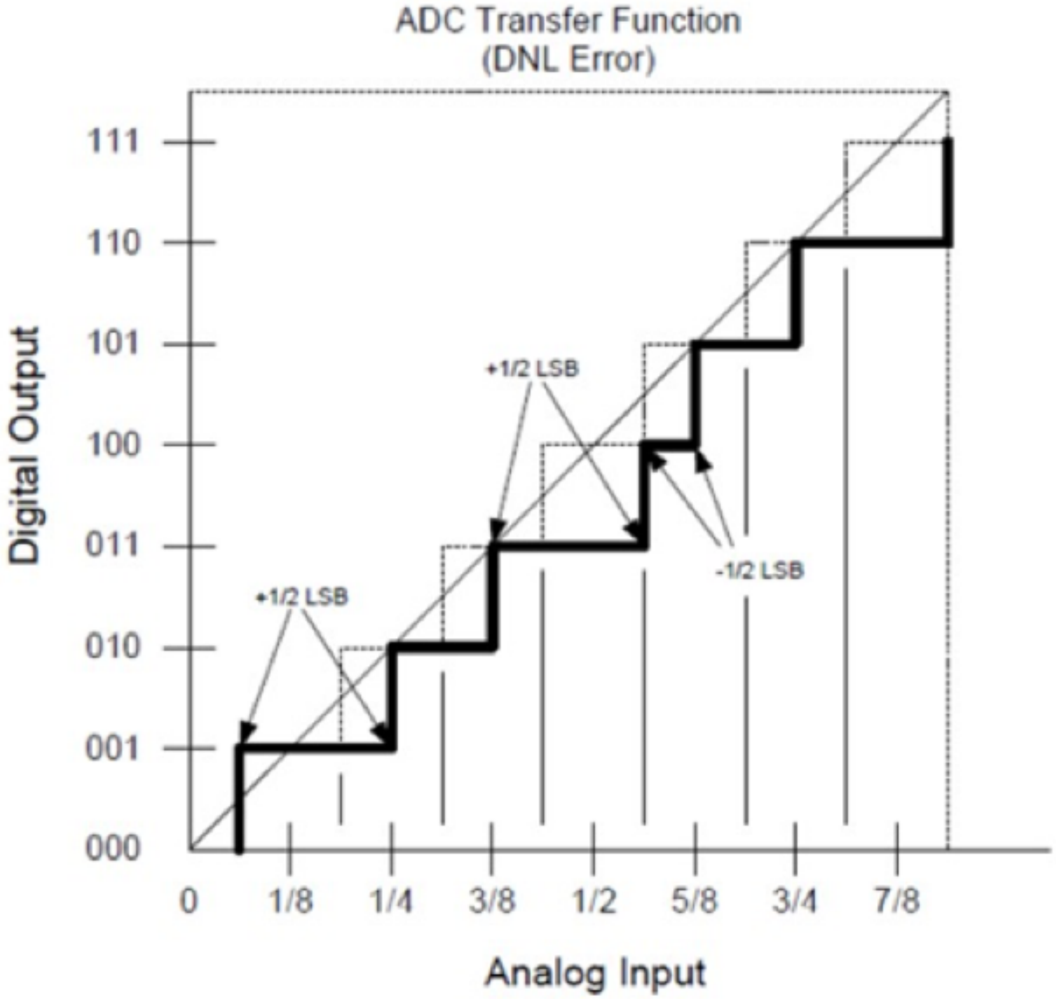
source: Renesas DevCon2015
Mitch Ferguson - ADC Specifications

ADC CHARACTERISTICS

Differential non-linearity (DNL)

The ideal transfer function is shown as the dotted line.

Actual transfer function is shown in bold line.
DNL causes wider or narrower code widths. Also, increases quantization noise.



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ADC IMPLEMENTATIONS

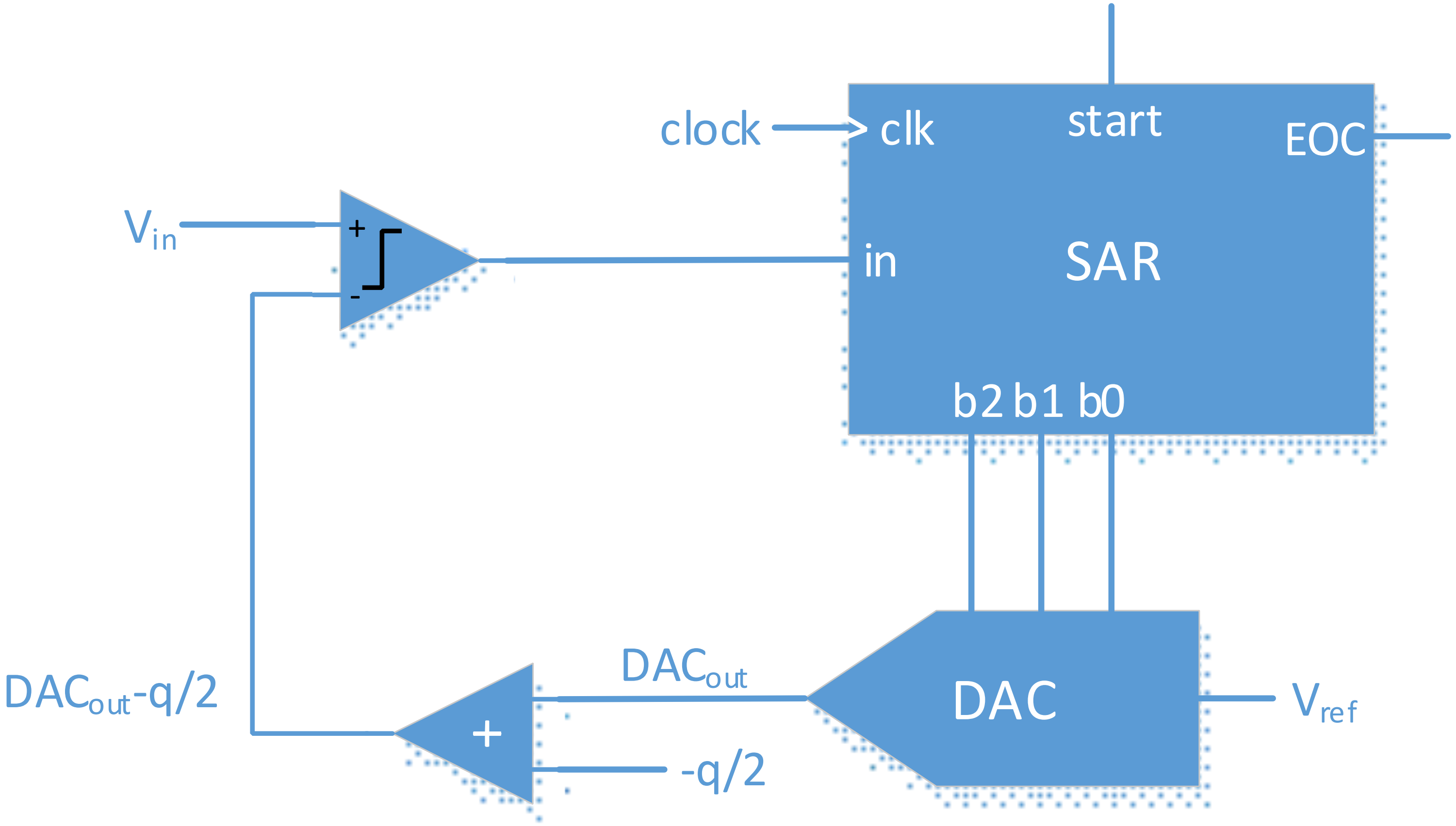
The most common ADC architectures (topologies) are:

Description
It is the fastest but also the one that requires the most circuitry (2^N comparators and resistors).
Two ADCs in sequence, the first resolves the MSb and the second the LSb.
Resolves bit-by-bit, thus, requiring a single comparator. Takes N clock cycles to generate the result.
Based on sigma-delta modulation, it is a 1-bit ADC that tracks the signal. It is based on oversampling, digital filtering and decimation.
Uses a single comparator whose reference voltage is a ramp. Counts the number of clock pulses to the ramp to reach the value of the input signal.
Integrates the input signal then integrates -Vref until the result of the integration reaches 0. Measures the time for the -Vref integration which is proportional to the amplitude of Vin.

SAR ADC

A SAR ADC (Successive Approximation Register Analog-to-Digital Converter) is based on a SAR, a Digital-to-Analog Converter and a Comparator.

The basic operation is to sequentially compare in input value to half of the analog range, decide if the input is in the upper or lower half, store this bit of information and move to the next comparison.



source: Authors

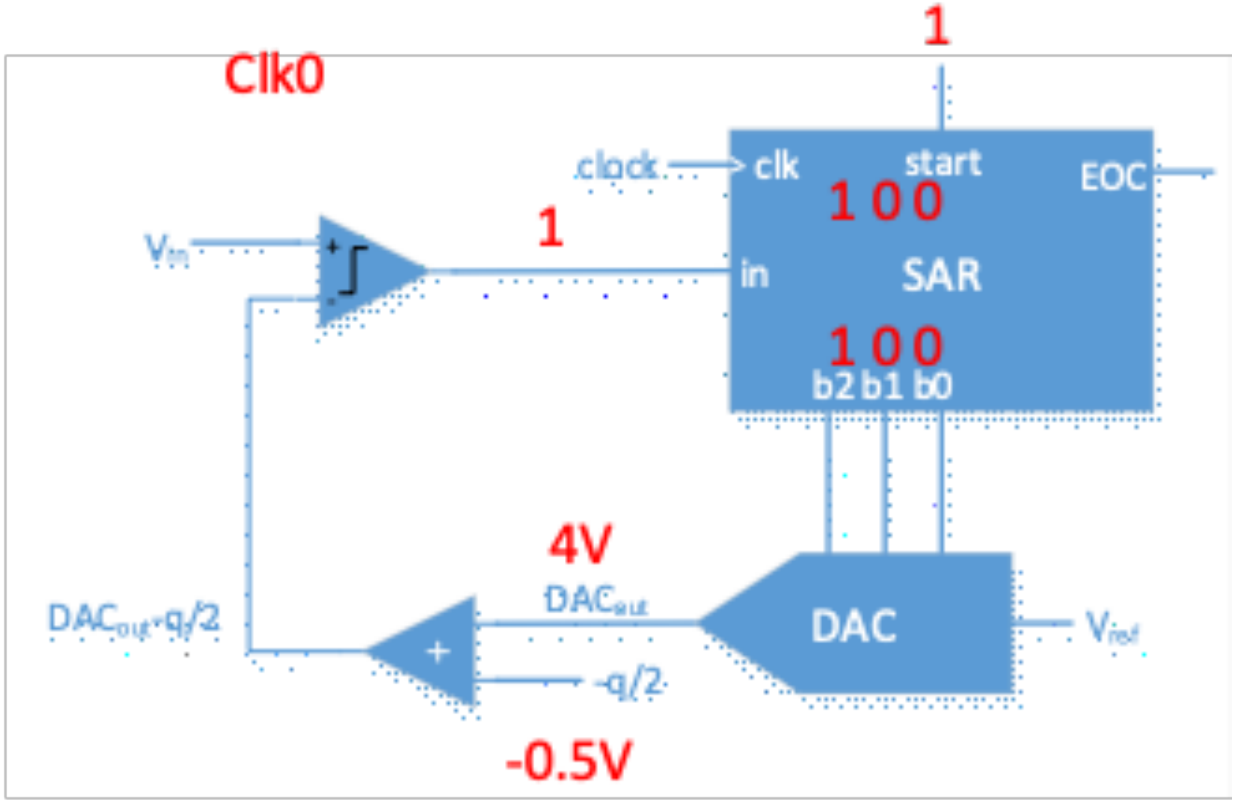
OPERATION OF THE SAR ADC

The same example as in the slide Quantization.
Vin = 3.8V, Vref = 8V, 3-bit ADC.

On the first clock cycle (Clk0):

- The SAR consists of a Shift Register (top) and a register holding the partial results (bottom).
- The start input of SAR is 1, this sets the first bit of the Shift Register in the SAR.
- The bit of the shift-register that is set, is used to compose the current reference value.
- The output 100 of the SAR is converted by the DAC to 4V, producing a 3.5V reference.
- The 3.8V input is compared to the 3.5V reference producing a 1 at the output of the comparator.

This is the MSb of the result that is latched in the SAR at the start of Clk1.



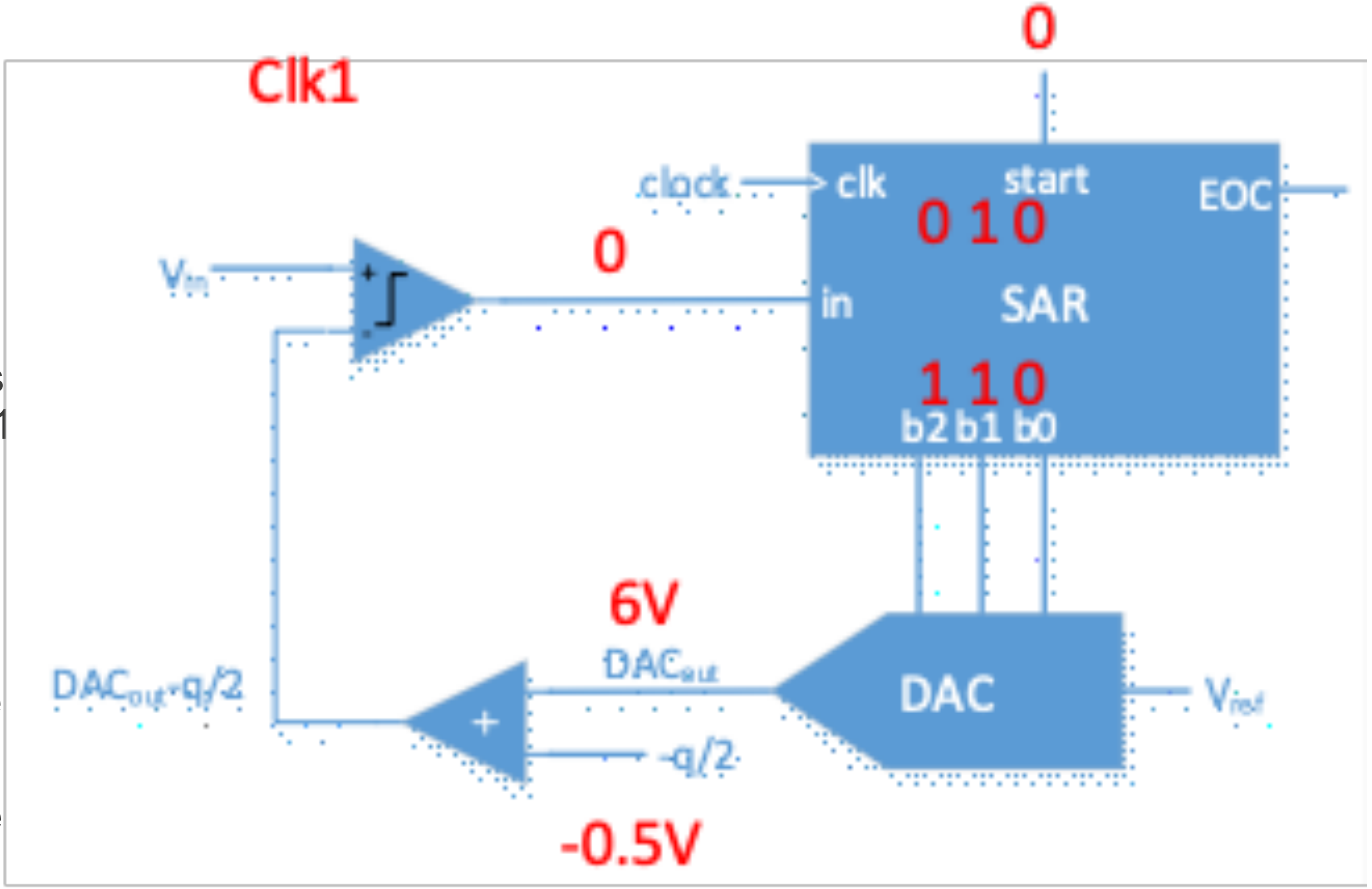
source: Authors

OPERATION OF THE SAR ADC

On the second clock cycle (Clk1):

- The start input of SAR is 0.
- The SARs Shift Register shifted the 1 bit to the next position.
- The partial result register holds a 1 at b2 that was latched at the start of the cycle, while b1 holds a 1 from the middle bit of the shift-register.
- The output 110 of the SAR is converted by the DAC to 6V, producing a 5.5V reference.
- The 3.8V input is compared to the 5.5V reference producing a 0 at the output of the comparator.

This is the next bit of the result that is latched in the SAR at the start of Clk2.



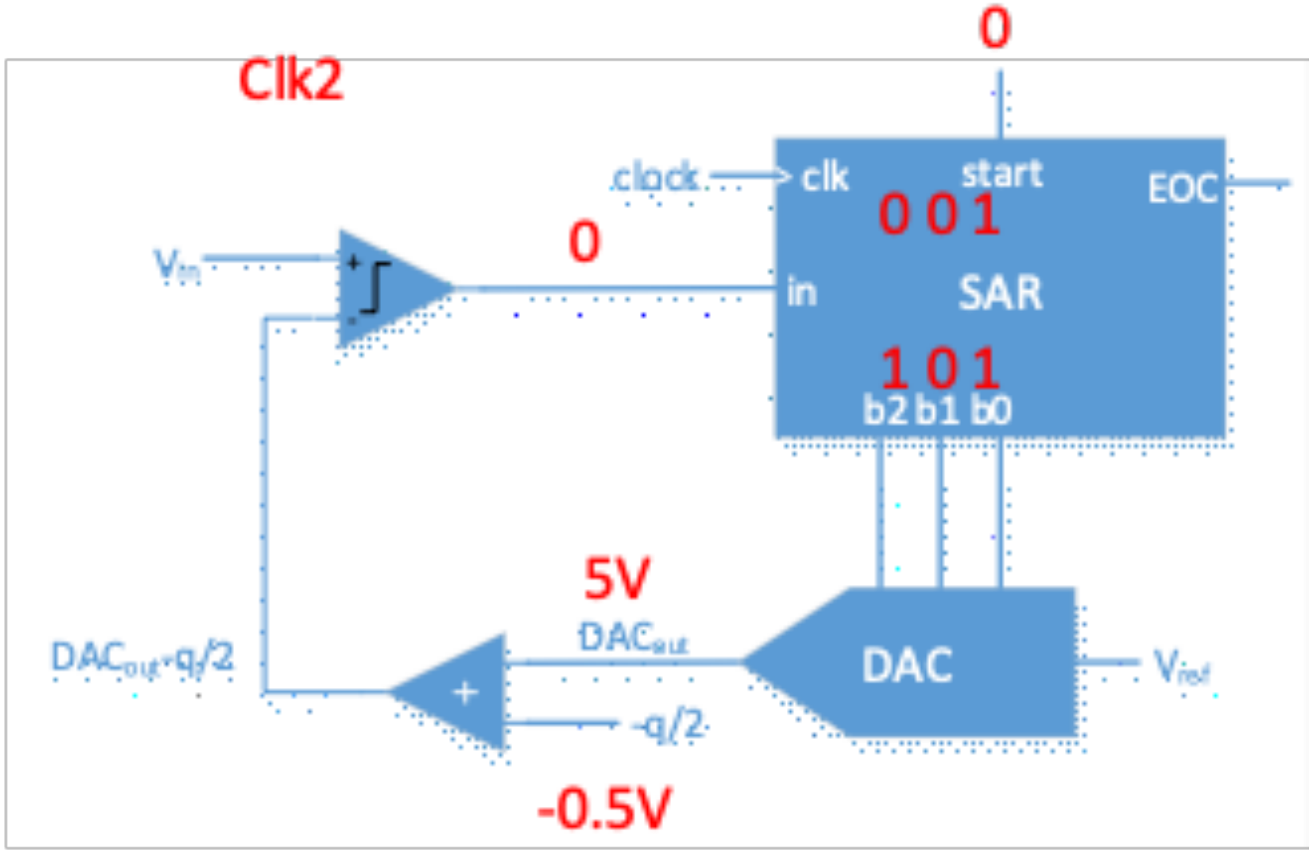
source: Authors

OPERATION OF THE SAR ADC

On the third clock cycle (Clk2):

- The start input of SAR is 0.
- The SARs Shift Register shifted the 1 bit to the next position.
- The partial result register holds a 10 at b2 b1 from the two previous comparisons,
  while b0 holds a 1 from the last bit of the shift-register.
- The output 101 of the SAR is converted by the DAC to 5V, producing a 4.5V reference.
- The 3.8V input is compared to the 4.5V reference producing a 0 at the output of the comparator.

This is the next bit of the result that is latched in the SAR at the start of the next clock

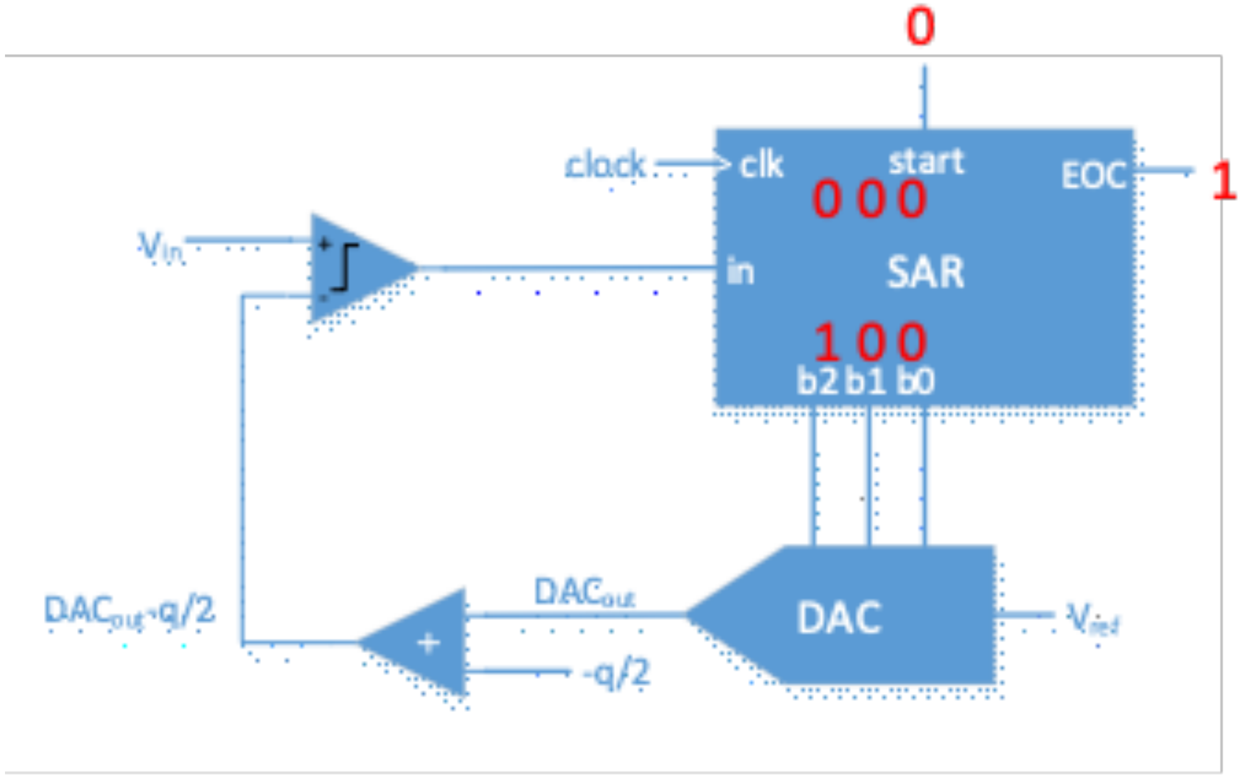


source: Authors

OPERATION OF THE SAR ADC

On the next clock cycle the result is available.

- The last bit of the shift-register is shifted out to EOC (end-of-conversion).
- The result of the conversion is presented at b2 b1 b0 that hold the results of the three previous comparisons.



source: Authors

DIGITAL TO ANALOG CONVERSION

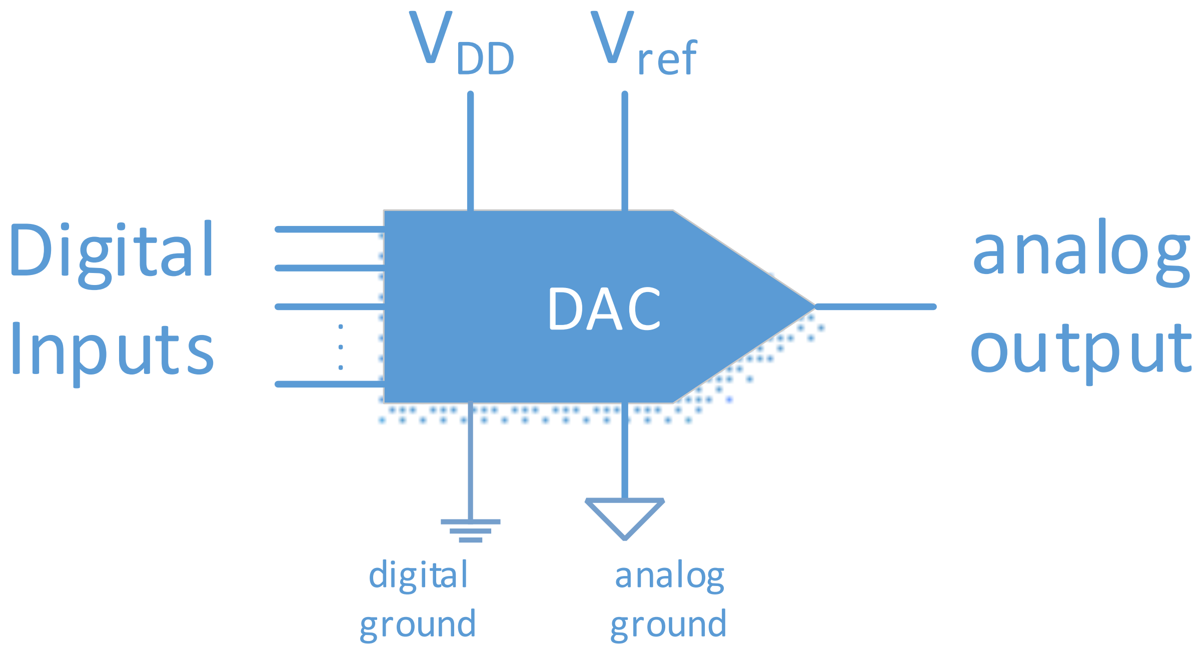
The Digital to Analog Converter (DAC) performs the opposite conversion of the ADC, i.e. it converts a digital value into the corresponding analog value according to the formula:

$$Analog\ output\ (V) = \frac{Digital\ Value}{2^N} V_{ref}$$

for an N-bit DAC whose input value is *Digital Value* and its analog reference voltage is $\mathrm{V}_{\mathrm{ref}}$

DIGITAL TO ANALOG CONVERSION

The schematics symbol for a DAC is:

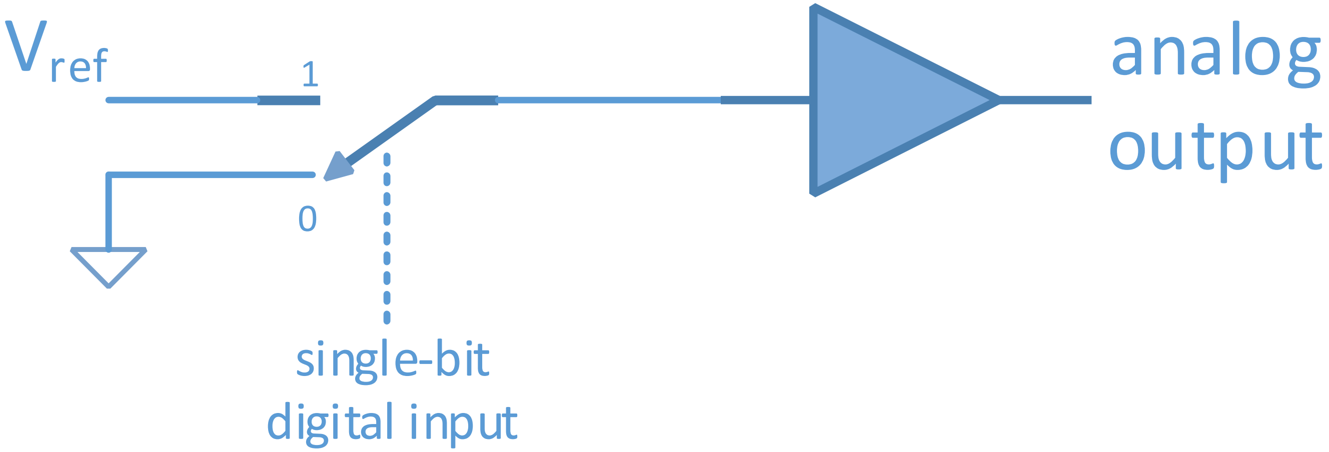


The number of digital input lines is N for an N-bit DAC.

source: Authors

SINGLE-BIT DIGITAL TO ANALOG CONVERTER

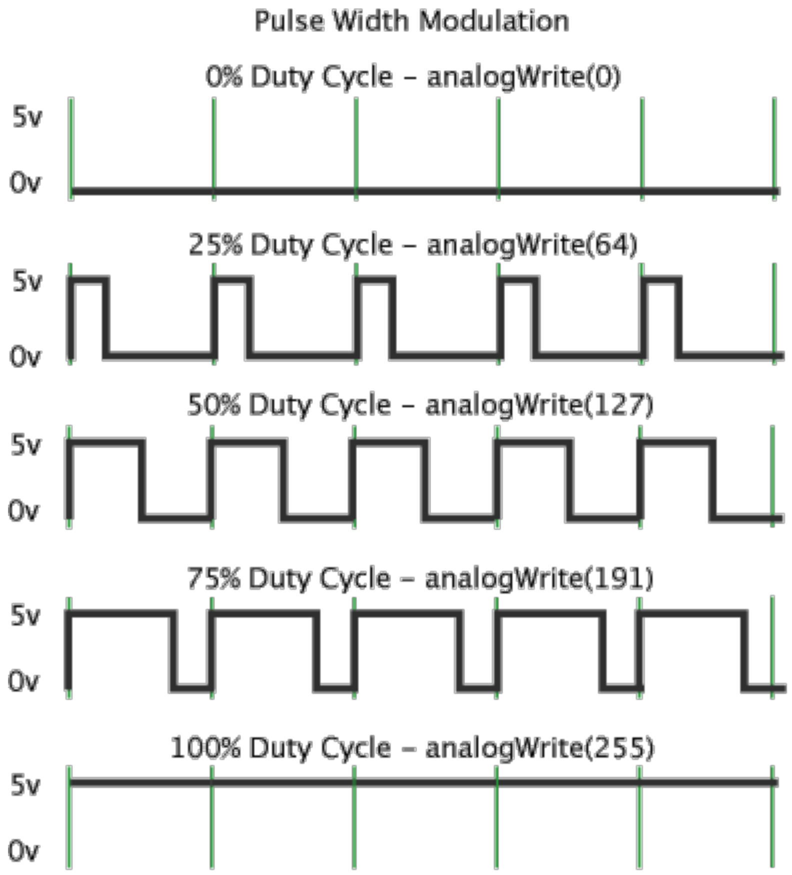
A single-bit DAC is the simplest form of a DAC. A single switch, which is controlled by the digital input, either connects the input of the analog amplifier to Vref or to ground. Hence, the possible analog output values are either 0 or Vref.

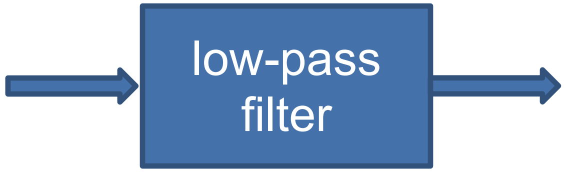


source: Authors

USING A PWM AS A DAC

The effect of 5 different duty cycles after passing a low-pass filter whose cutoff frequency is much lower than the PWM frequency.





low-pass filter

0 V

1.25 V

2.5 V

3.75 V

5V

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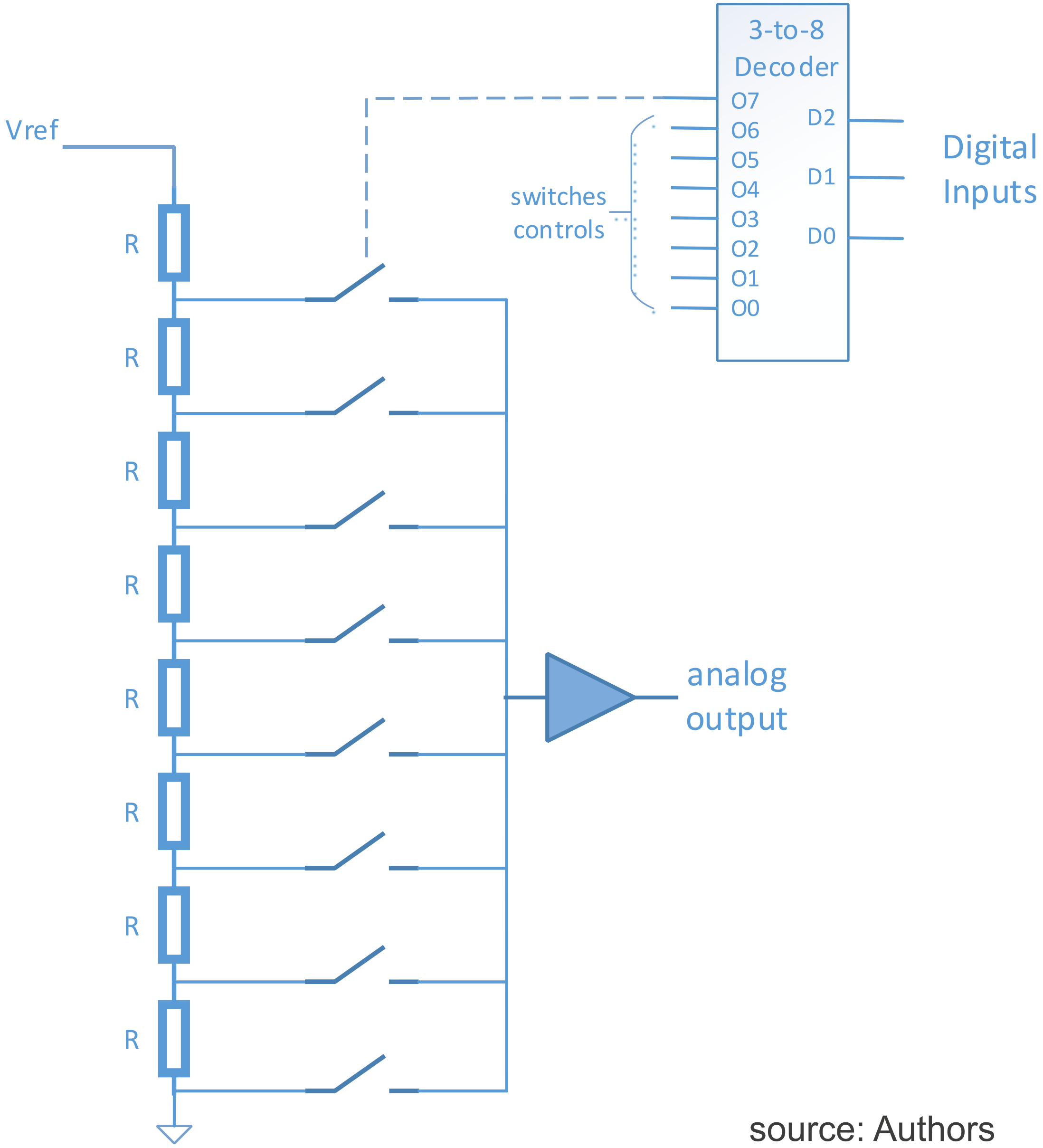
USING A PWM AS A DAC

The topology presented is a Kelvin Divider DAC, also called a string DAC. Among its advantages are its monotonicity and low-glitch.

It requires 2^N resistors and switches for an N-bit DAC, which makes it impractical for a larger number of bits.



source: Authors

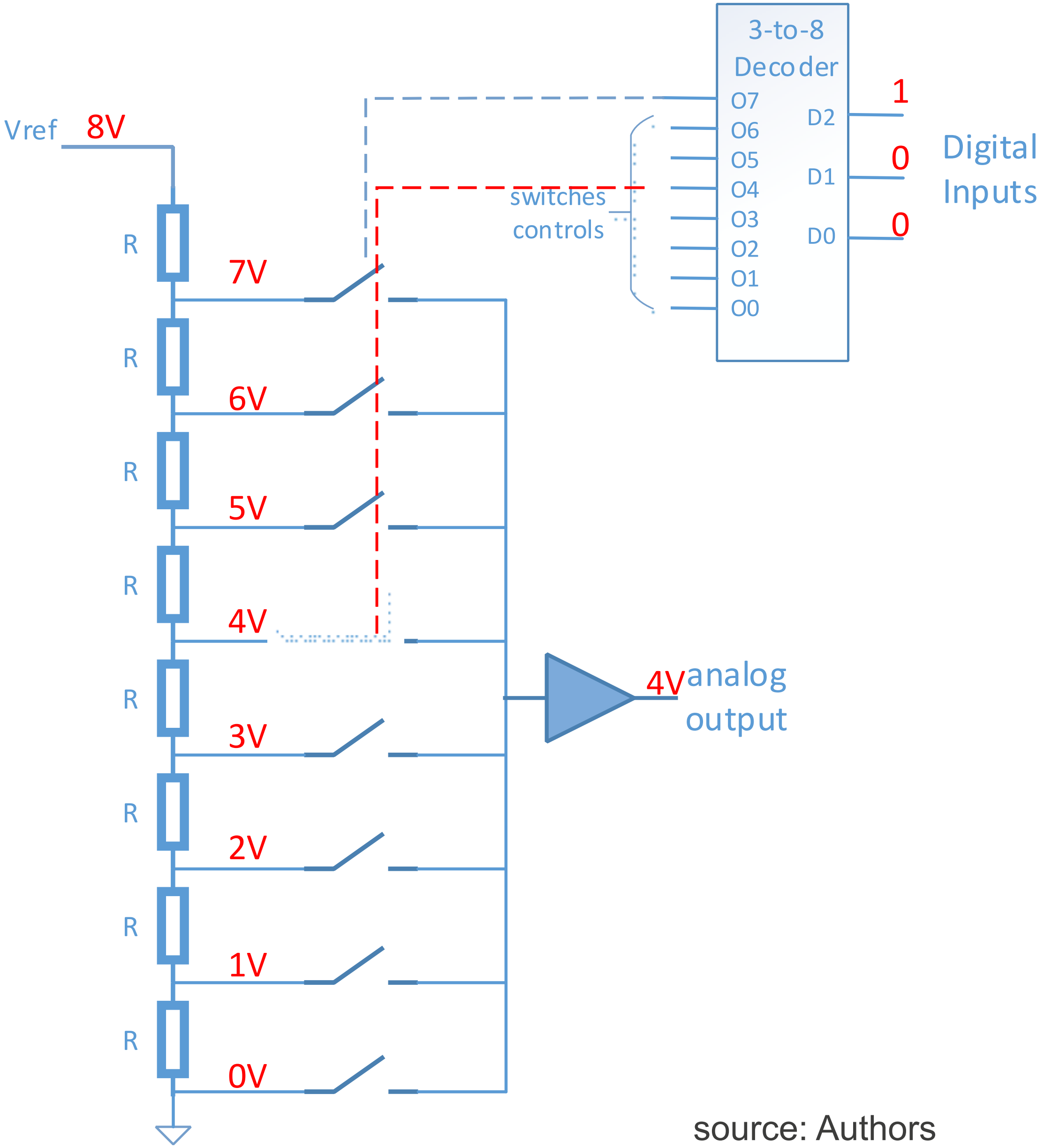
OPERATION OF THE 3-BIT DAC

In this example, Vref is 8V and the digital input has the value 4 (100b).

Output O4 of the decoder is active and commands the corresponding switch. The resistor string has values 1V apart

at each of its taps.

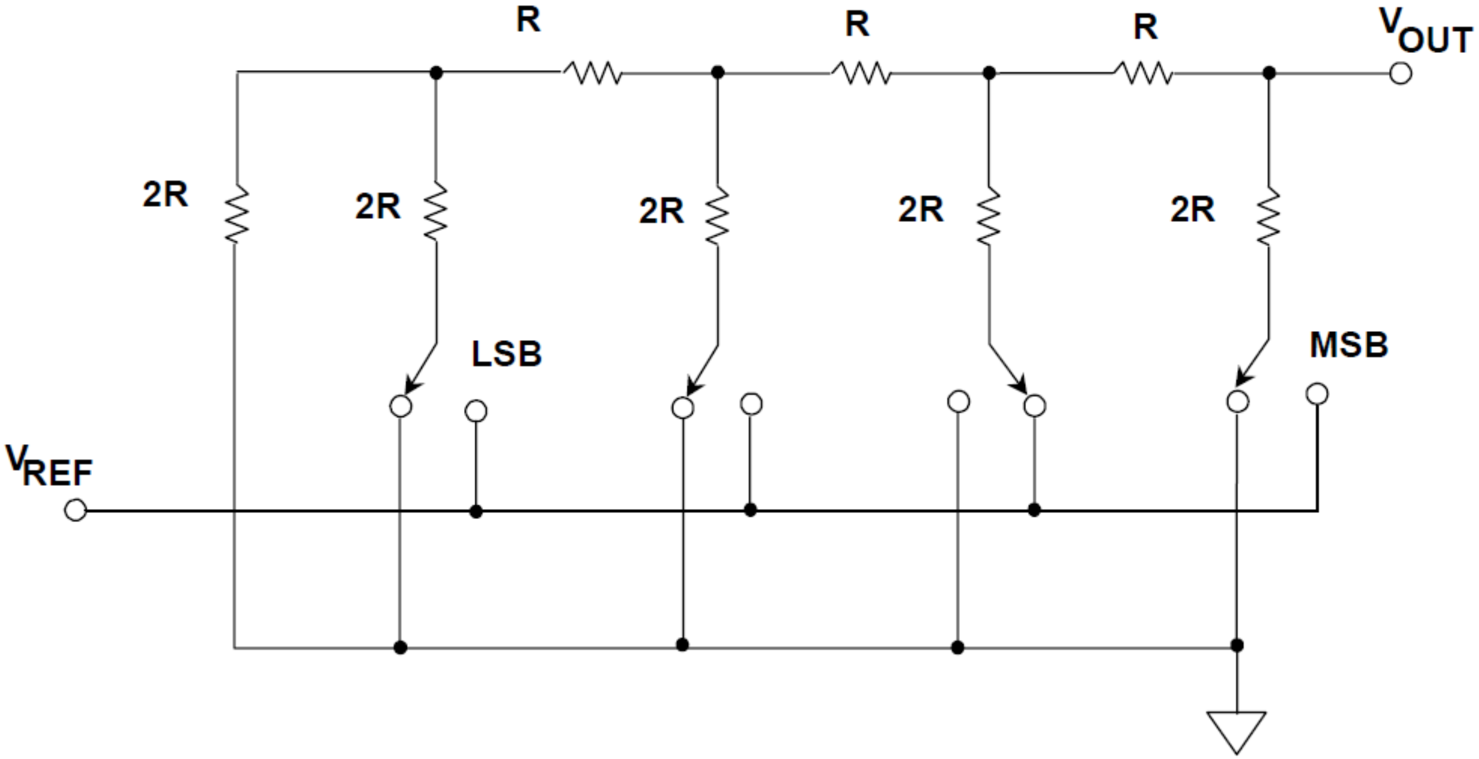
The output analog amplifier simply provides isolation, avoiding that the impedance of the load affects the analog value at the taps of the resistor string.



source: Authors

R2R LADDER DAC

The R2R resistor ladder topology has the advantages of requiring only 2N resistors in the ladder and the values of these resistors are either R or 2R, avoiding components with a significant difference in value, as would be the case for the binary-weighted DAC that requires values of R, 2R, 4R, 8R, 16R, ...



source:
The Data Conversion Handbook, Edited by Walt Kester, Analog Devices Inc.

DAC CASE STUDY THE S7G2 DAC

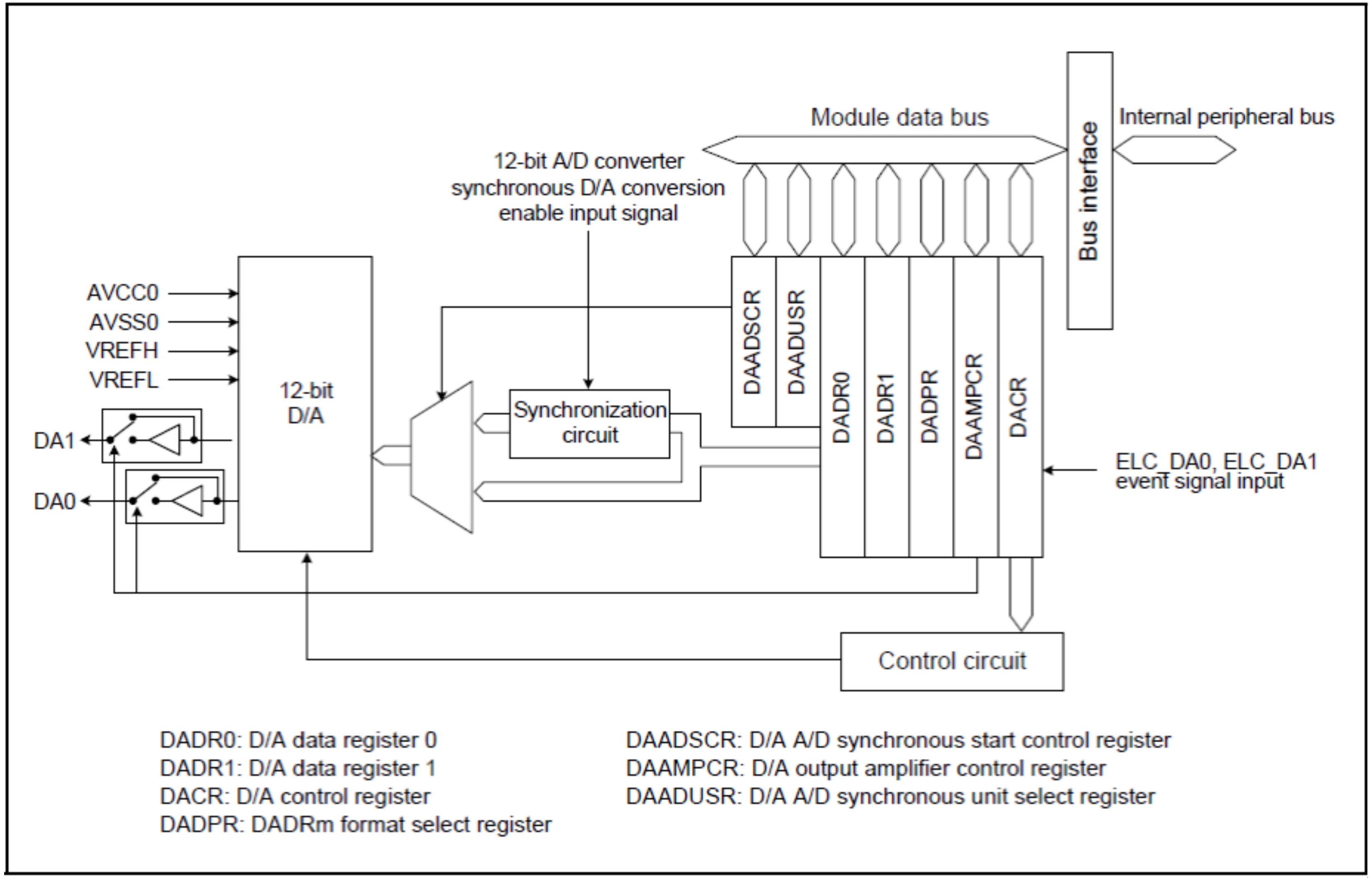
Characteristics:

- Two 12-bit DACs available: DAC0 and DAC1,
- The 12-bit value present at the DADRi register is converted to an analog value of $V\_(ref\ )\ DADRi/4096$,
- Output amplifier is available, may be enabled under SW control,
- DAC operation may be synchronized to ADC1,
- DAC conversion may be started by an ELC event.

DAC CASE STUDY THE S7G2 DAC

DAC0 and DAC1

block diagram



DADR0: D/A data register 0
DADR1: D/A data register 1
DACR: D/A control register
DADPR: DADRm format select register

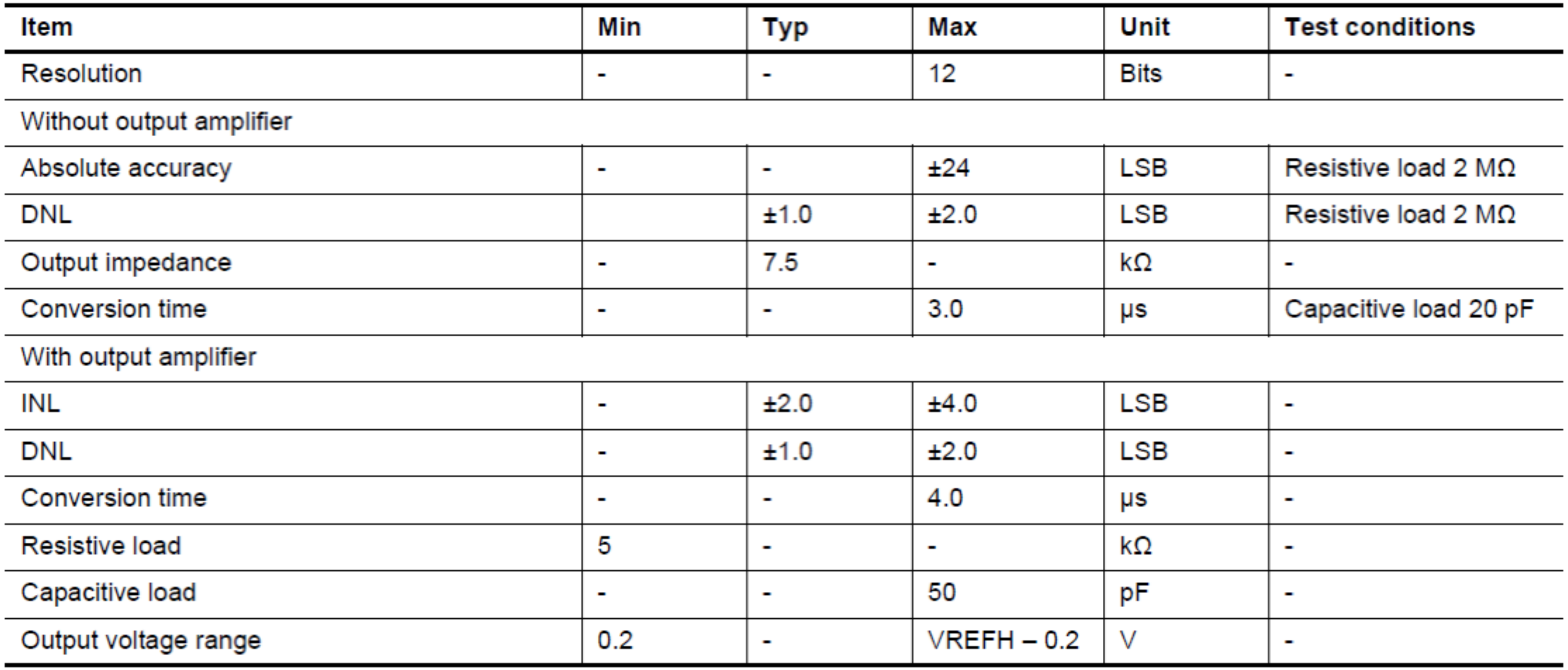
DAADSCR: D/A A/D synchronous start control register
DAAMPCR: D/A output amplifier control register
DAADUSR: D/A A/D synchronous unit select register

source: Renesas S7G2 user's manual

DAC CASE STUDY THE S7G2 DAC

Renesas S7G2 DAC characteristics:

Table 2.43 D/A conversion characteristics



Item	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	Bits	-
Without output amplifier					
Absolute accuracy	-	-	±24	LSB	Resistive load 2 MΩ
DNL		±1.0	±2.0	LSB	Resistive load 2 MΩ
Output impedance	-	7.5	-	kΩ	-
Conversion time	-	-	3.0	µs	Capacitive load 20 pF
With output amplifier					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
Conversion time	-	-	4.0	µs	-
Resistive load	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.2	-	VREFH – 0.2	V	-

source: Renesas S7G2 datasheet

Renesas.com